Laduree 15.6" Intel Crescent Bay

UMA/DIS Co-lay Schematic

Broadwell-U 15W TDP
nVidia N16S-GM 16W

REV:1

2015-02-13

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Cover Page*		
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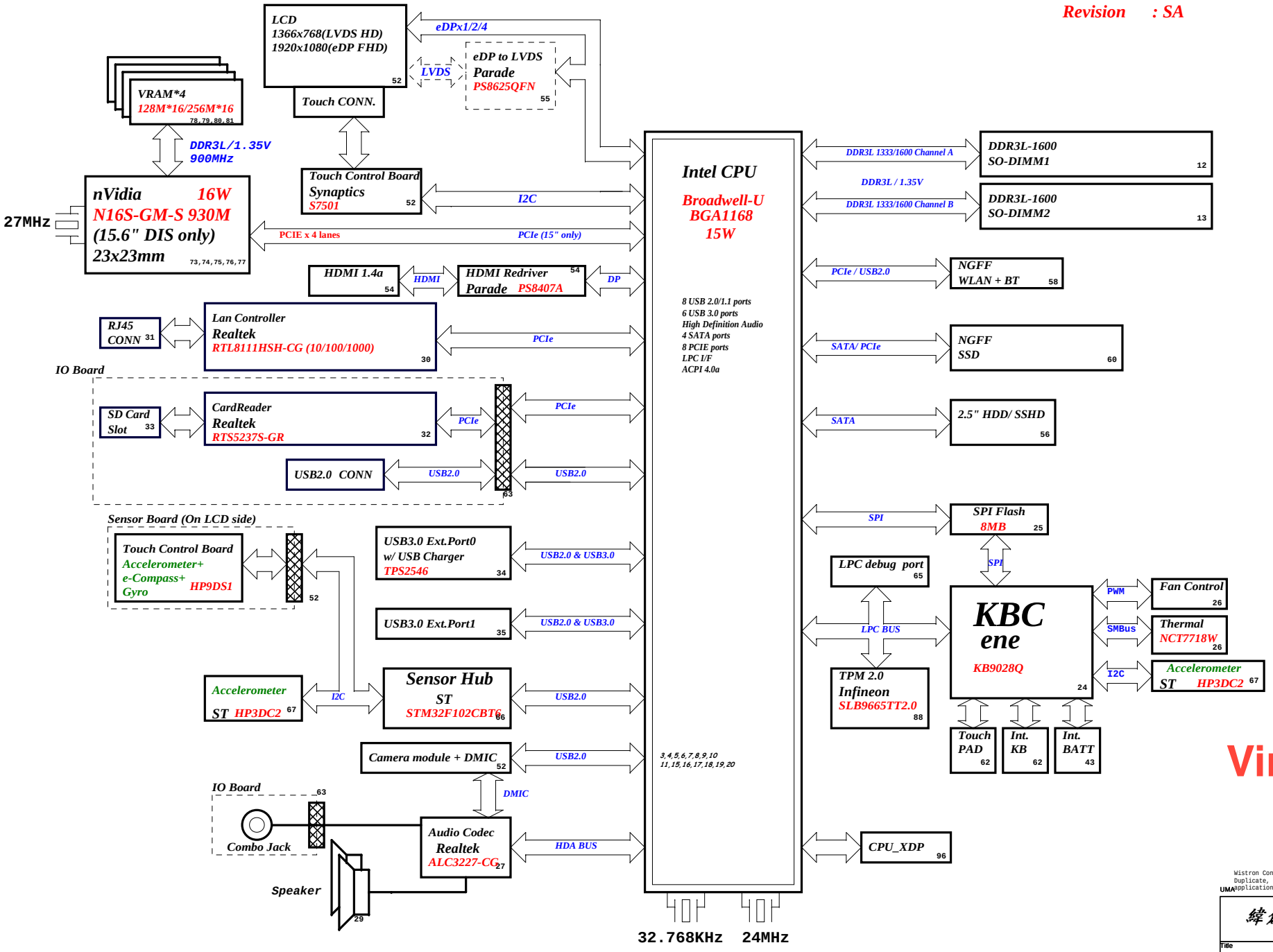
Date: Friday, February 13, 2015	Sheet 1 of 102	

Laduree 15.6" Block Diagram

Project code : 4PD048010001
PCB P/N : 14257
Revision : SA



CHARGER HPA02224RGRR 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC TPS51624RSMR 46,47	
INPUTS	OUTPUTS
DCBATOUT	CPU_CORE

SYSTEM DC/DC RT8068AZQWID 51	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0

SYSTEM DC/DC SY8208DQNC 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_LAN

SYSTEM DC/DC TPS51716RUKR 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_PWR

VGA RT8179CGQW 80,81	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

VGA RT8068AZQWID SY8208DQNC 82	
INPUTS	OUTPUTS
3D3V_S5	1D8V
DCBATOUT	0D95V

PCB LAYER

L1: TOP	L5: GND/PWR
L2: GND	L6: BOTTOM
L3: Signal	
L4: Signal	

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Title: Block Diagram

Size: Custom	Document Number: Laduree-BDW 15.6"	Rev: 1

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SSID = CPU

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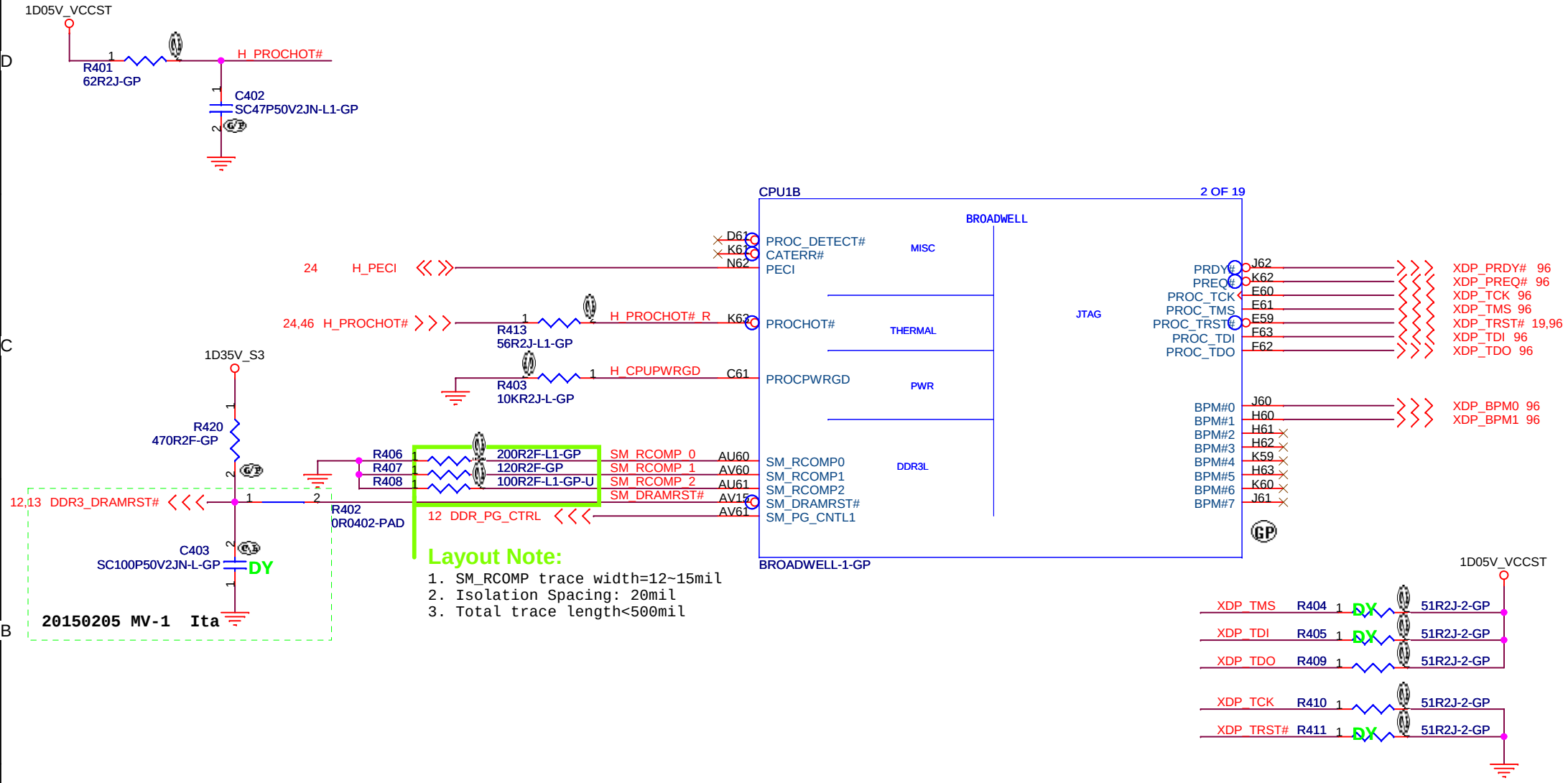
Title	***CPU (Reserved)***	
Size A4	Document Number **Laduree-BDW 15.6"**	Rev **1**
Date: Friday, January 30, 2015	Sheet 3 of 102	

SSID = CPU



Layout Note:

1. SM_RCOMP trace width=12~15mil
2. Isolation Spacing: 20mil
3. Total trace length<500mil

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Title: **CPU (THERMAL/CLOCK/PM)**

Size	Document Number	Rev
A4	Laduree-BDW 15.6"	1

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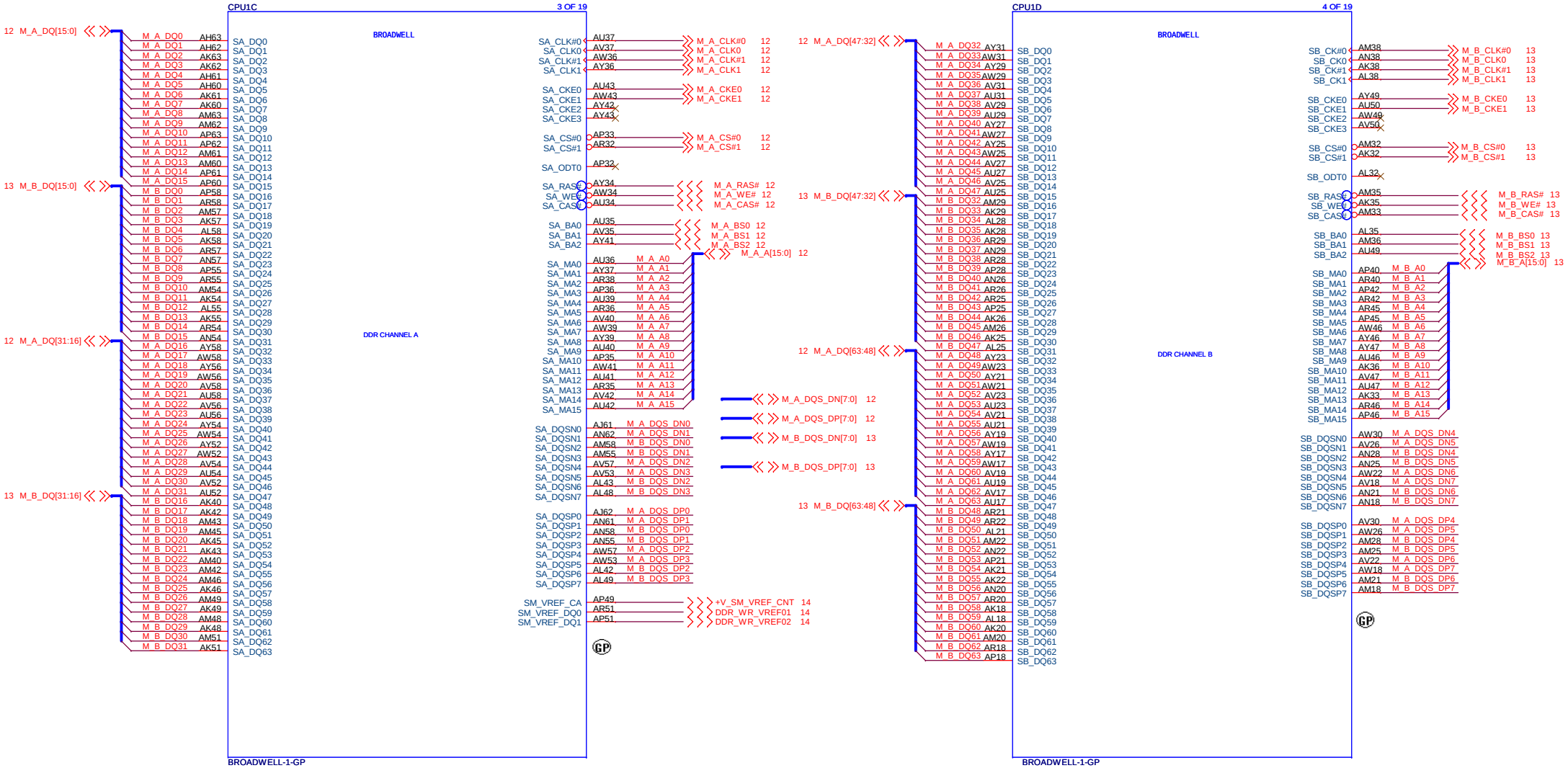
SSID = CPU



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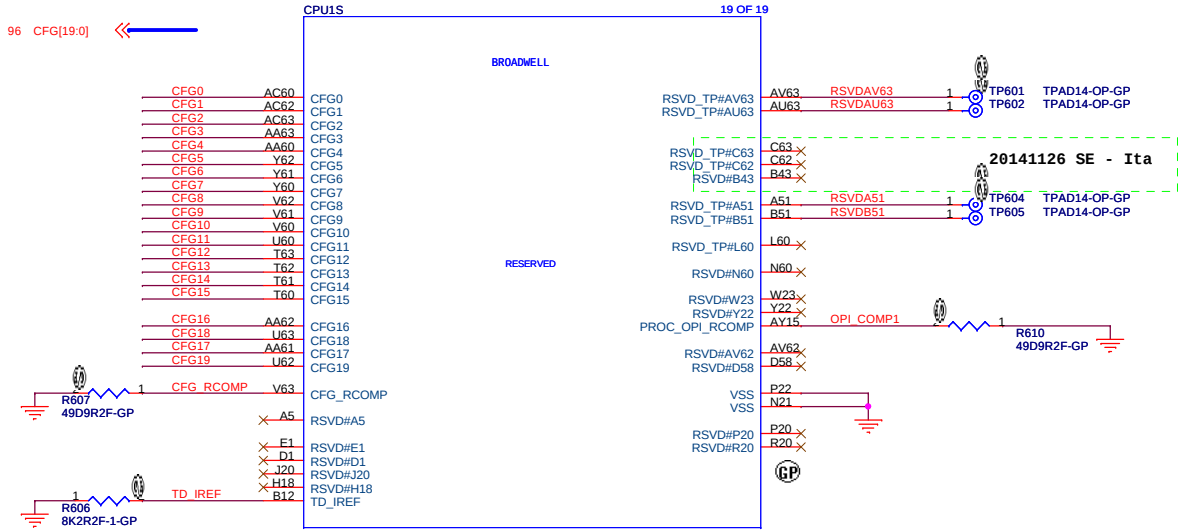
Title: **CPU (DDR)**

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 5 of 102

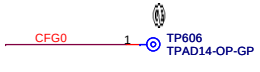
SSID = CPU



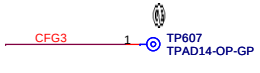
7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

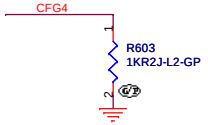
- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected



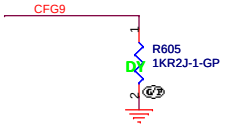
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified)	Default Value	✓
CFG[0]		Connect a series 1 kΩ resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.		



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT



NO SVID PROTOCOL CAPABLE VR CONNECTED
0:NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOTGENERATE (OR RESPOND TO) SVID ACTIVITY
1:VRS SUPPORTING SVID PROTOCOL ARE PRESENT

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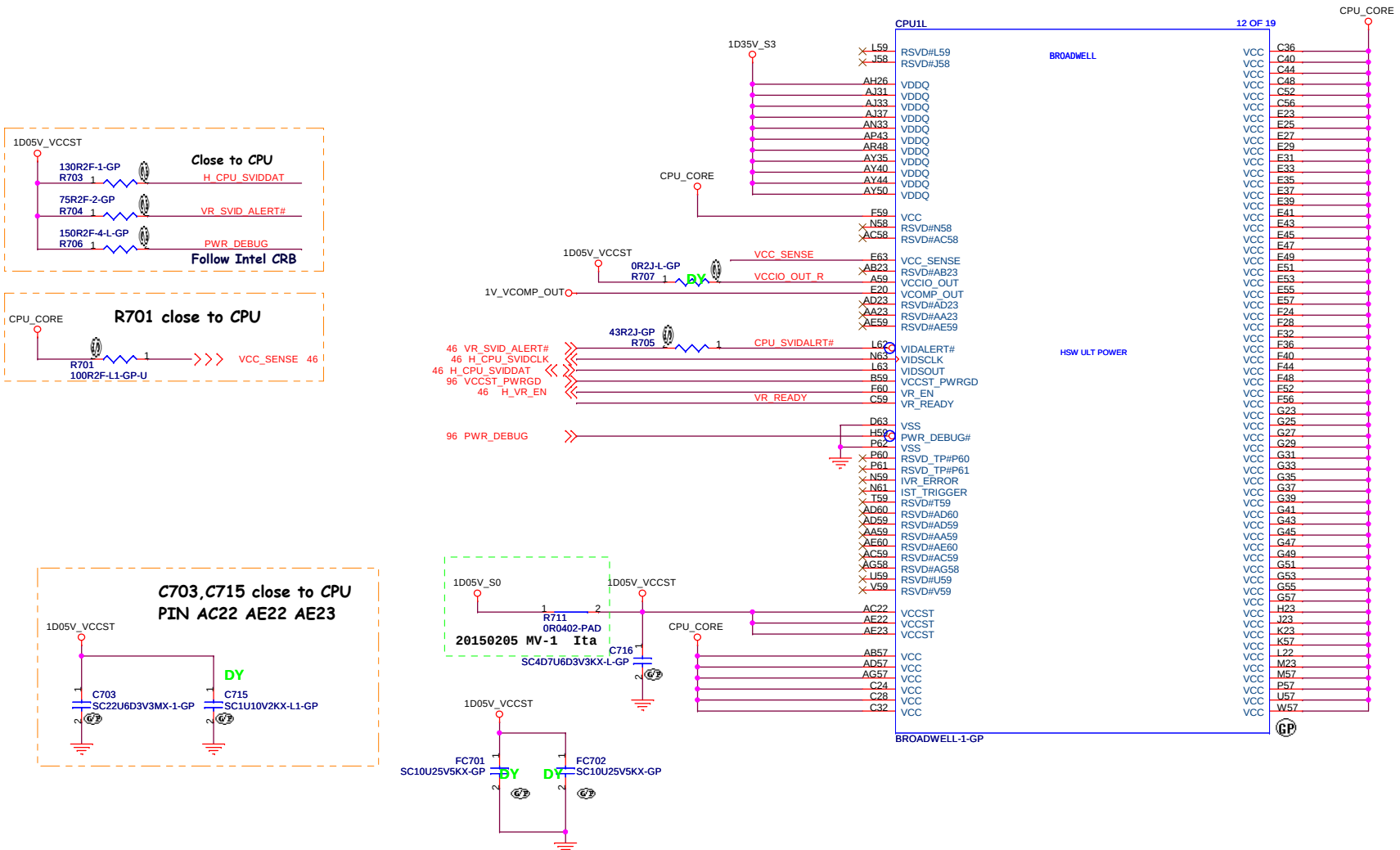
Title: **CPU (CFG)**

Size	Document Number	Rev
Custom	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 6 of 102

SSID = CPU



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Title: **CPU (VCC_CORE)**

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

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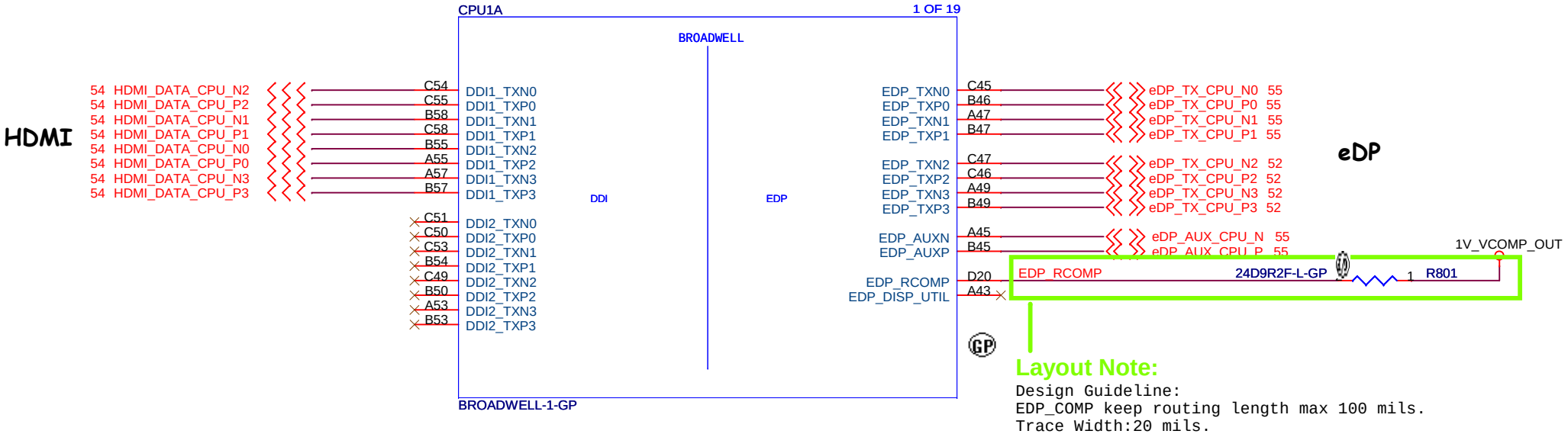
SSID = CPU



Layout Note:

Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Bit Rate	Supports (in # of lanes)	Peak Bandwidth
1.62 Gb/s	4	4 x 162 MB/s = 648 MB/s
5.4 Gb/s	4	4 x 540 MB/s = 2160 MB/s
2.7 Gb/s	4	4 x 270 MB/s = 1080 MB/s

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Title: ***CPU (DDI/EDP)***

Size: A4 | Document Number: **Laduree-BDW 15.6"** | Rev: 1

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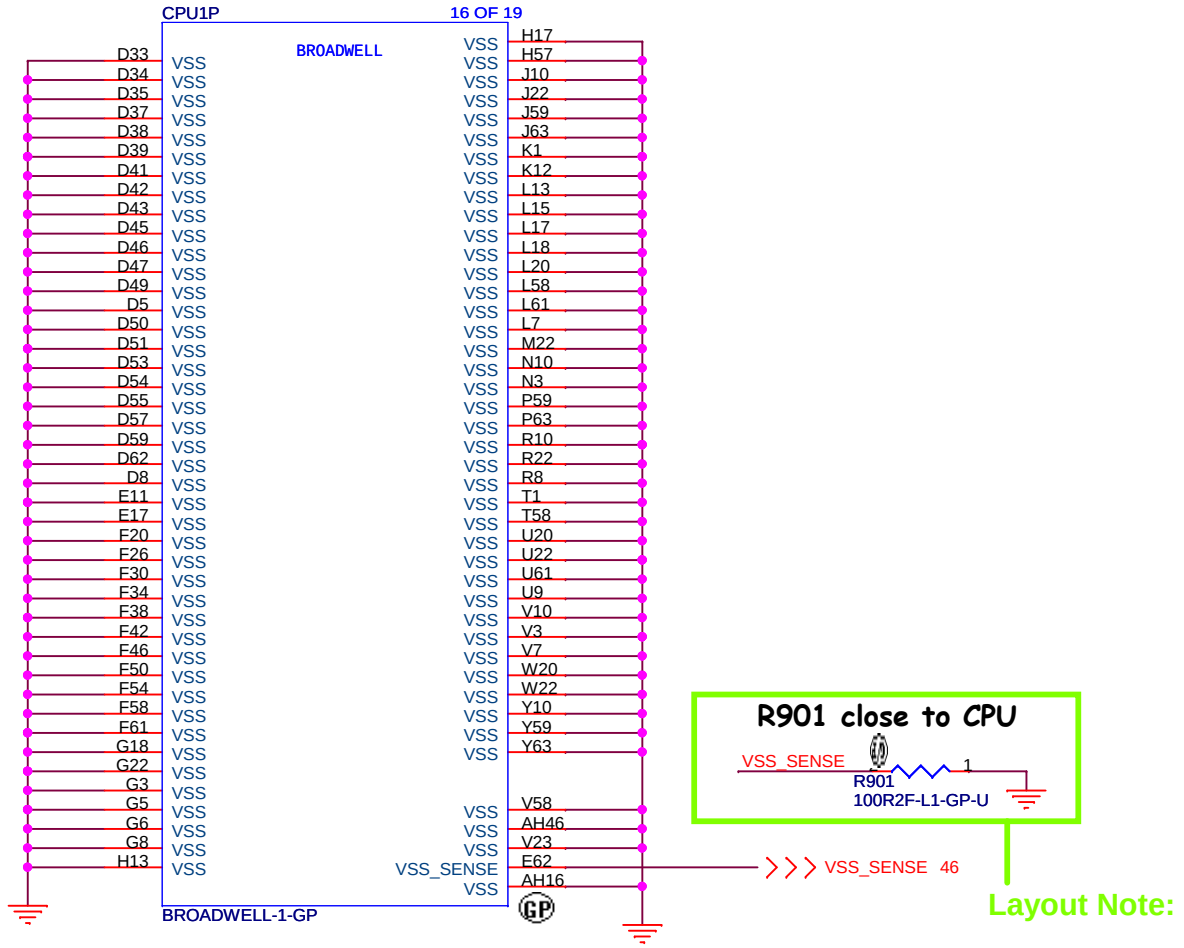
SSID = CPU



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Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

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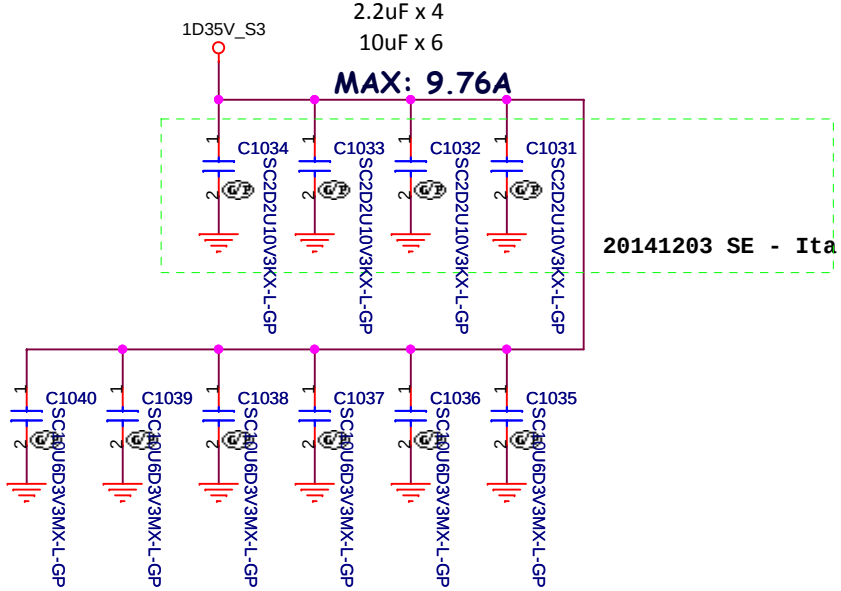
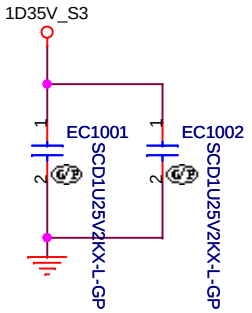
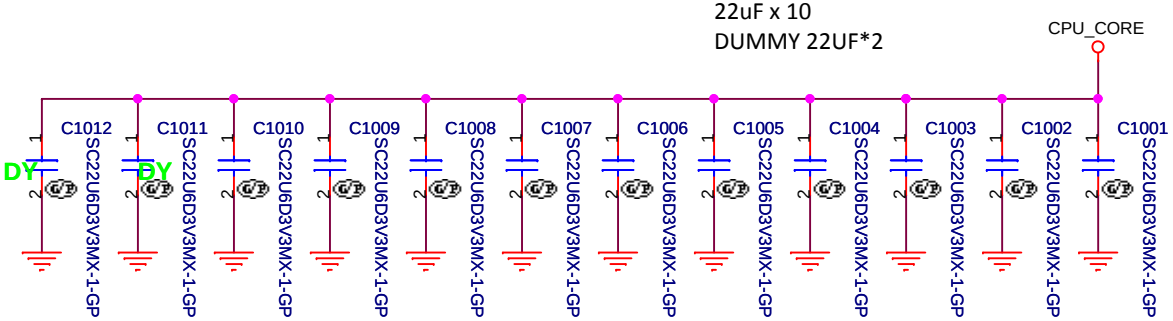
SSID = MCP

1D35V_S3
2.2uF x 4
10uF x 6
MAX: 9.76A

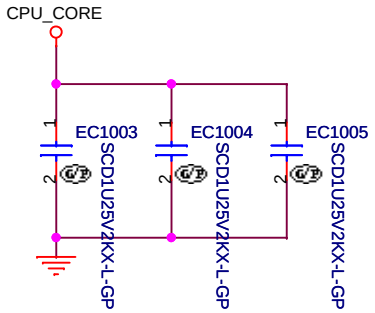


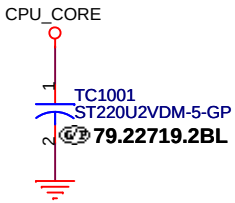


CPU_CORE
22uF x 10
DUMMY 22UF*2



20141204 SE - Ita change back





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Title: ***CPU (Power CAP1)***

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

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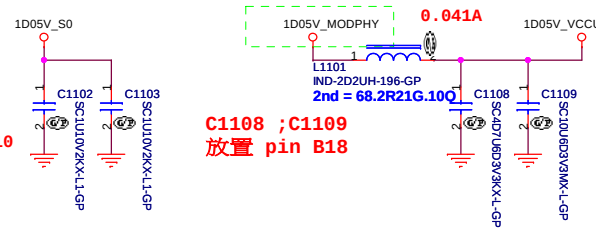
擺放電容的位置請參考Page 21
每個位置如下

MAX: 1.92A

20141022 SC - Terry

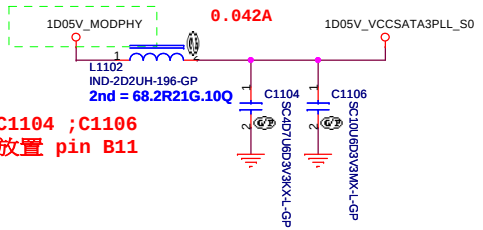


C1102;C1103
放置pin K9 L10

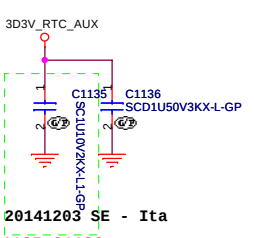
20141022 SC - Terry

C1108 ;C1109
放置 pin B18

20141022 SC - Terry

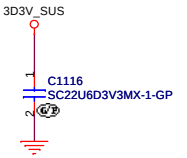


C1104 ;C1106
放置 pin B11



20141203 SE - Ita

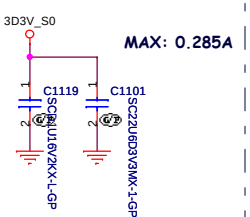
C1135;C1136
放置 pin AG10



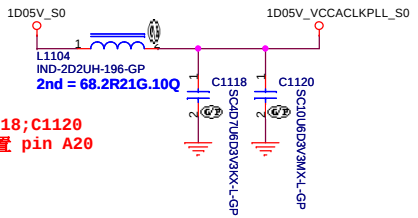
20141204 SE - Ita change back

C1116放置 pin AC9, AA9

MAX: 0.285A

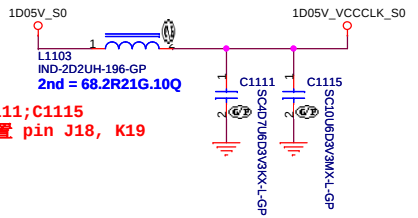


C1101 放置 pin V8
C1119 放置 pin K14



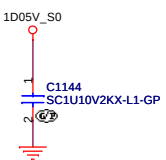
C1118;C1120
放置 pin A20

MAX: 3.51A

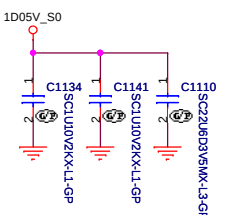


C1111;C1115
放置 pin J18, K19

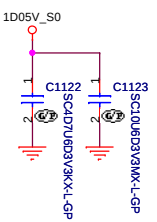
20141204 SE - Ita change back



C1144
放置 pin AE9



C1110 放置 pin J11
C1134 C1141 放置 pin J11, AE8



C1122;C1123
放置 pin AA21

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Title: CPU (Power CAP2)

Size: A3 | Document Number: Laduree-BDW 15.6" | Rev: 1

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SSID = MEMORY

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM Memory Connectivity and Topology
ODT Signal Connectivity and Support
For DDR3L SODIMM designs, Intel recommends ODT signals not to be routed between CPU and DIMM on platform, leave ODT at CPU as no-connect (open), and tie DIMM ODT to VDDQ through FET and resistor. The reason for this additional ODT-control circuitry on the platform is to save power dissipation by turning off VDDQ to VTT path during low power states, as ODT signal is terminated to VTT through RTT on SODIMM. The ODT value for DDR3L SODIMM 1-DPC platform will be encoded in the write command and use RTT_NOM = Off and RTT_WR = (60,120) Ohm.
- CPU ODT output would be NOCON
- SODIMM ODT input should be tied to VDDQ through a FET and a resistor to support low power states.

DIMM1

DDR3-204P-306-GP
062.10011.0461

H = 4mm

RN1202 SRN10KJ-5-GP

DDR3L SODIMM ODT GENERATION

U2G2 74AUP1G07GW REV-1

R2H1 220K 5% 402
R2H2 2.0M 5% EMPTY 402
R2G6 0 5% EMPTY 402
R2G5 0 5% 402
C2G13 0.1UF 20% 16V 402

R2G2 66.5 402 1% M_A_DIM0_ODT0
R2G1 66.5 402 1% M_A_DIM0_ODT1
R4G3 66.5 402 1% M_B_DIM0_ODT0
R4G4 66.5 402 1% M_B_DIM0_ODT1

Q2H1 M_A_B_DIMM_ODT

Thermal EVENT

R1204 10K/R2J-L2-GP

Q1202 Q1203限用於84.05067.031
因為此刻Vth為1V

Q1202 DMN5L06K-7-GP 84.05067.031
Q1203 DMN5L06K-7-GP 84.05067.031
R1212 220KR2J-L2-GP

ODT resistor must be 66.5 ohm

R1208 R1209 R1210 R1211 66D5R2F-GP

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

Place these caps close to VTT1 and VTT2.

Close DIMM1 VREF_CA pin

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Title: DDR3-SODIMM1
Size: Custom | Document Number: Laduree-BDW 15.6" | Rev: 1
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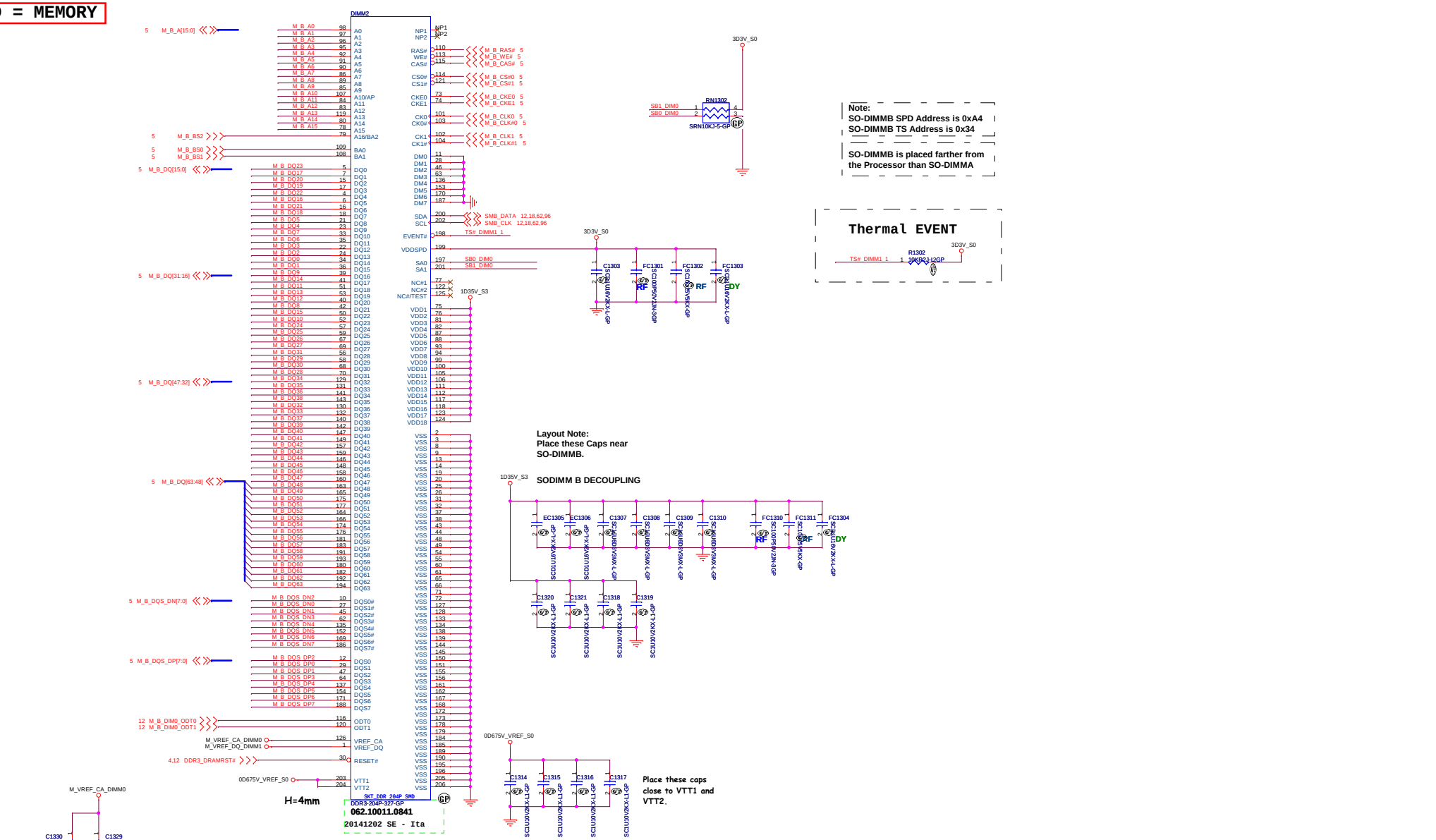
SSID = MEMORY



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Title: DDR3-SODIMM2

Size	Document Number	Rev
A2	Laduree-BDW 15.6"	1

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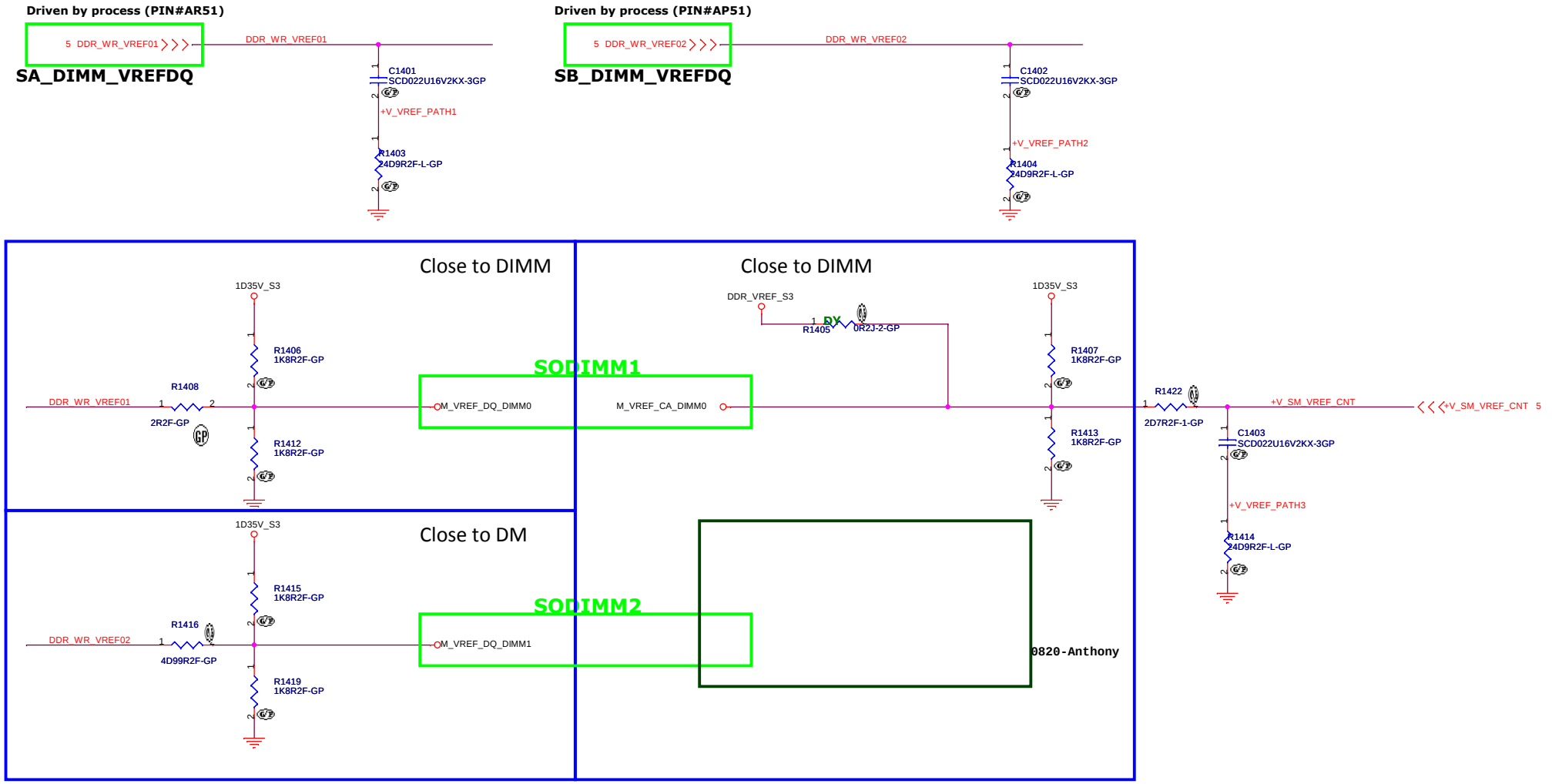
VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation



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Title: ***M1 & M3 Implementation***

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

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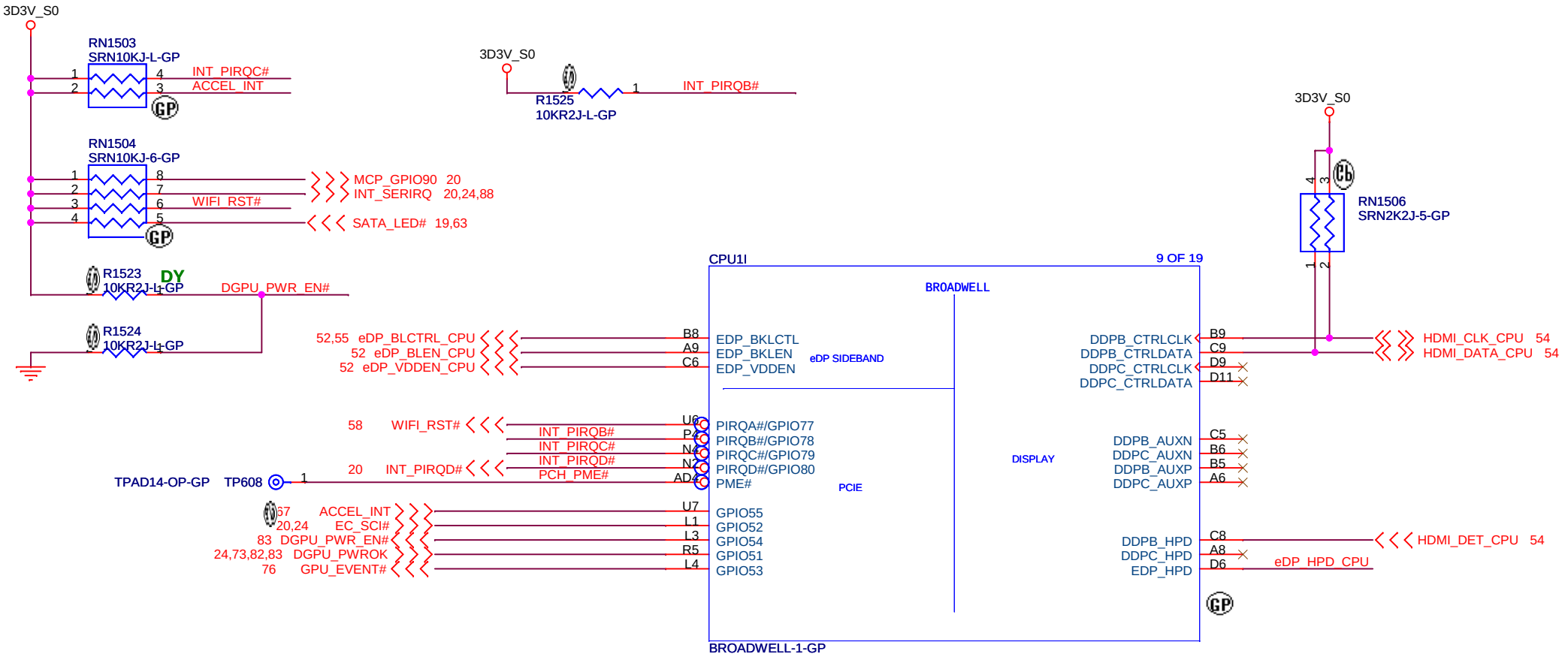
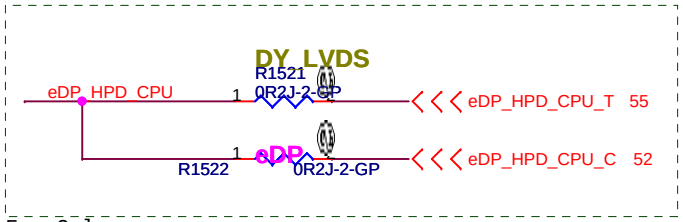
SSID = CPU





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Title: ***CPU(EDP SIDEBAND/GPIO/DDI)***

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

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SSID = PCH

73 PCIE_RXN[5..8]
73 PCIE_RXP[5..8]
PCIE_TXP[5..8] 73
PCIE_TXN[5..8] 73

dGPU
LAN
WLAN
Cardreader

CPU1K 11 OF 19 BROADWELL

PCIE_RXN5 F10 PERN5_L0
PCIE_RXP5 E10 PERP5_L0
PCIE_TXN5 C1605 1 SCD22U10V2KX-L1-GP PCIE_TXN5_C C23 PETN5_L0
PCIE_TXP5 C1606 1 SCD22U10V2KX-L1-GP PCIE_TXP5_C C22 PETP5_L0
PCIE_RXN6 F8 PERN5_L1
PCIE_RXP6 E8 PERP5_L1
PCIE_TXN6 C1607 1 SCD22U10V2KX-L1-GP PCIE_TXN6_C B23 PETN5_L1
PCIE_TXP6 C1608 1 SCD22U10V2KX-L1-GP PCIE_TXP6_C A23 PETP5_L1
PCIE_RXN7 H10 PERN5_L2
PCIE_RXP7 G10 PERP5_L2
PCIE_TXN7 C1613 1 SCD22U10V2KX-L1-GP PCIE_TXN7_C B21 PETN5_L2
PCIE_TXP7 C1614 1 SCD22U10V2KX-L1-GP PCIE_TXP7_C C21 PETP5_L2
PCIE_RXN8 E6 PERN5_L3
PCIE_RXP8 F6 PERP5_L3
PCIE_TXN8 C1615 1 SCD22U10V2KX-L1-GP PCIE_TXN8_C B22 PETN5_L3
PCIE_TXP8 C1616 1 SCD22U10V2KX-L1-GP PCIE_TXP8_C A21 PETP5_L3

30 PCIE_RX_CPU_N3 G11 PERN3
30 PCIE_RX_CPU_P3 F11 PERP3
30 PCIE_TX_LAN_N3 C1619 1 SCD1U16V2KX-L-GP PCIE_TX_CPU_N3 C29 PETN3
30 PCIE_TX_LAN_P3 C1620 1 SCD1U16V2KX-L-GP PCIE_TX_CPU_P3 B30 PETP3
58 PCIE_RX_CPU_N4 F13 PERN4
58 PCIE_RX_CPU_P4 G13 PERP4
58 PCIE_TX_WLAN_N4 C1621 1 SCD1U16V2KX-L-GP PCIE_TX_CPU_N4 B29 PETN4
58 PCIE_TX_WLAN_P4 C1622 1 SCD1U16V2KX-L-GP PCIE_TX_CPU_P4 A29 PETP4
63 PCIE_RX_CPU_N1 G17 PERN1/USB3RN3
63 PCIE_RX_CPU_P1 F17 PERP1/USB3RP3
63 PCIE_TX_CARD_N1 C1623 1 SCD1U16V2KX-L-GP PCIE_TX_CPU_N1 C30 PETN1/USB3TN3
63 PCIE_TX_CARD_P1 C1624 1 SCD1U16V2KX-L-GP PCIE_TX_CPU_P1 C31 PETP1/USB3TP3
F15 PERN2/USB3RN4
G15 PERP2/USB3RP4
B31 PETN2/USB3TN4
A31 PETP2/USB3TP4

1D05V_VCCUSB3PLL_S0
3K01R2F-3-GP R1601 1
PCIE_COMP
E15 RSVD#E15
E13 RSVD#E13
A27 PCIE_RCOMP
B27 PCIE_IREF

BROADWELL-1-GP

USB2N0 AN8 USB_CPU_PN0 35
USB2P0 AM8 USB_CPU_PP0 35
USB2N1 AR7 USB_CPU_PN1 34
USB2P1 AT7 USB_CPU_PP1 34
USB2N2 AR8 USB_CPU_PN2 63
USB2P2 AP8 USB_CPU_PP2 63
USB2N3 AR10 USB_CPU_PN3 58
USB2P3 AT10 USB_CPU_PP3 58
USB2N4 AM15
USB2P4 AL15
USB2N5 AM13
USB2P5 AN13
USB2N6 AP11 USB_CPU_PN6 52
USB2P6 AN11 USB_CPU_PP6 52
USB2N7 AR13 USB_CPU_PN7 91
USB2P7 AP13 USB_CPU_PP7 91

USB3RN1 G20 USB30_RX_CPU_N1 34
USB3RP1 H20 USB30_RX_CPU_P1 34
USB3TN1 C33 USB30_TX_CPU_N1 34
USB3TP1 B34 USB30_TX_CPU_P1 34
USB3RN2 E18 USB30_RX_CPU_N2 34
USB3RP2 F18 USB30_RX_CPU_P2 34
USB3TN2 B33 USB30_TX_CPU_N2 34
USB3TP2 A33 USB30_TX_CPU_P2 34

USBRBIAS# AJ10 USB_RBIAS 22D6R2F-L1-GP R1611 1
USBRBIAS AJ11
RSVD#AN10 AN10
RSVD#AM10 AM10

OC0#/GPIO40 AL3 USB_OC#
OC1#/GPIO41 AT1
OC2#/GPIO42 AH2
OC3#/GPIO43 AV3
3D3V_SUS
R1602 10KR2J-L-GP 1 2

USB Table

Pair	Device
0	USB3.0 Port 1(CHG)
1	USB3.0 Port 2
2	USB2.0 Port 1(IO BD)
3	WLAN(Bluetooth)
4	N/A
5	N/A(Touch screen)
6	CCD
7	Sensor Hub

USB3.0 (CHG)

USB3.0

Layout Note:
1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:
1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

UMA

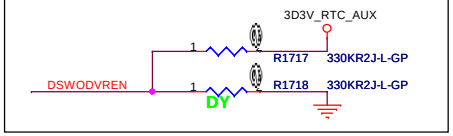
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

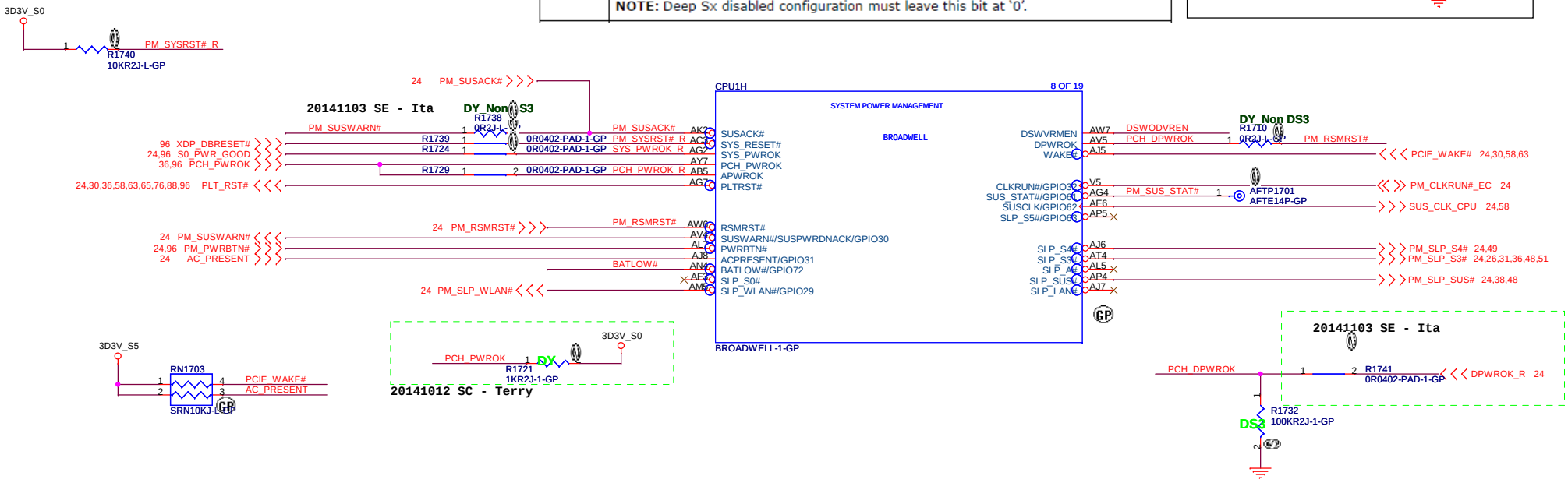
Title: CPU (PCI/USB)
Size: A3 | Document Number: Laduree-BDW 15.6" | Rev: 1
Date: Thursday, February 12, 2015 | Sheet 16 of 102

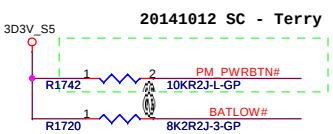
SSID = CPU

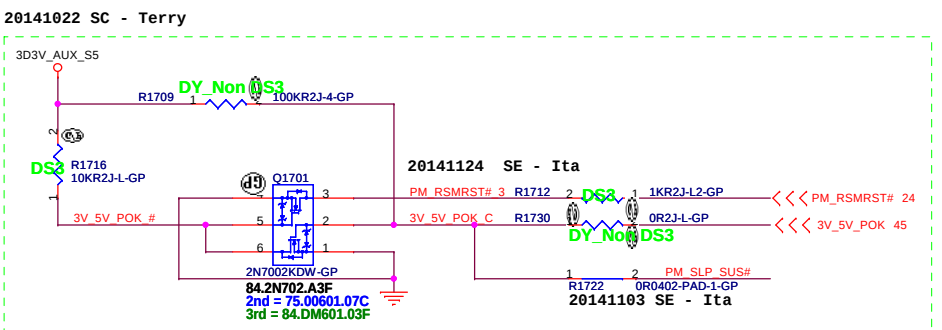
Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

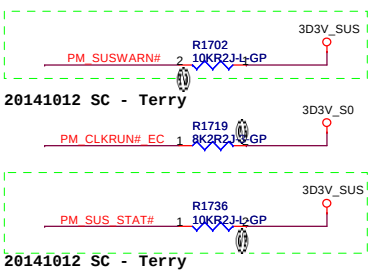
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled











UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DMI/FDI/PM)**

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 17 of 102

SSID = CPU

Close to CPU

3D3V_S0

RN1808 — SRN10KJ-6-GP
CLKREQ_SSD#
CARD_CLKREQ_CPU#
CK_REQ
20141107 SD - Ita
H_RCIN# 20,24

RN1812 — SRN10KJ-L-GP
WLAN_CLKREQ_CPU#
PEG_CLKREQ#
20141107 SD - Ita

Cardreader
63 CARD_CLK_CPU#
63 CARD_CLK_CPU
63 CARD_CLKREQ_CPU#

LAN
30 LAN_CLK_CPU#
30 LAN_CLK_CPU
20,30 LAN_CLKREQ_CPU#

WLAN
58 WLAN_CLK_CPU#
58 WLAN_CLK_CPU
58 WLAN_CLKREQ_CPU#

GPU PEG BUS
73 CLK_PCIE_VGA#
73 CLK_PCIE_VGA
73 PEG_CLKREQ#

CK_REQ
CLKREQ_SSD#
20141107 SD - Ita

CPU1F — 6 OF 19 — BROADWELL — CLOCK SIGNALS

C43 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
U2 PCIECLKRQ0#/GPIO18
B41 CLKOUT_PCIE_N1
A41 CLKOUT_PCIE_P1
Y5 PCIECLKRQ1#/GPIO19
C41 CLKOUT_PCIE_N2
B42 CLKOUT_PCIE_P2
AD1 PCIECLKRQ2#/GPIO20
B38 CLKOUT_PCIE_N3
C37 CLKOUT_PCIE_P3
N1 PCIECLKRQ3#/GPIO21
A39 CLKOUT_PCIE_N4
B39 CLKOUT_PCIE_P4
U5 PCIECLKRQ4#/GPIO22
B37 CLKOUT_PCIE_N5
A37 CLKOUT_PCIE_P5
T2 PCIECLKRQ5#/GPIO23

XTAL24_IN A25 CPU_XTAL_24M_IN
XTAL24_OUT B25 CPU_XTAL_24M_OUT
RSVD#K21 K21
RSVD#M21 M21
DIFFCLK_BIASREF C26 DIFFCLK_BIAS
TESTLOW_C35 C35 CLK_BUF_CKSSCD_N
TESTLOW_C34 C34 CLK_BUF_CKSSCD_P
TESTLOW_AK8 AK8 CLK_BUF_DOT96_P
TESTLOW_AL8 AL8 CLK_BUF_DOT96_N
CLKOUT_LPC_0 AN15 CLK_PCI_LPC_R
CLKOUT_LPC_1 AP15 CLK_PCI_TPM_R
CLKOUT_ITPXDP_N B35 PCIE_CLK_XDP_N 96
CLKOUT_ITPXDP_P A35 PCIE_CLK_XDP_P 96

BROADWELL-1-GP

CPU_XTAL_24M_IN — C1808 SC15P50V2JN-L-GP
R1807 1MR2J-L3-GP
X1801 XTAL-24MHZ-81-GP 82.30004.841
CPU_XTAL_24M_OUT — C1807 SC15P50V2JN-L-GP

3K01R2F-3-GP R1801 — 1D05V_VCCACLKPLL_S0

22R2J-2-GP R1804 — CLK_PCI_LPC 65
22R2J-2-GP R1802 — CLK_PCI_KBC 24, CLK_PCI_TPM 88
22R2J-2-GP R1803

RN1810 — SRN10KJ-L-GP
CLK_BUF_CKSSCD_N
CLK_BUF_CKSSCD_P

RN1811 — SRN10KJ-L-GP
CLK_BUF_DOT96_P
CLK_BUF_DOT96_N

Need very close to CPU

CLK_PCI_LPC — FC1801 DY SC4D7P50V2BN-GP
CLK_PCI_KBC — FC1802 DY SC4D7P50V2BN-GP
CLK_PCI_TPM — FC1803 DY SC4D7P50V2BN-GP

3D3V_S0 — RN1807 SRN2K2J-5-GP

Q1801 DN7002KDW-GP 84.2N702.A3F 2nd = 75.00601.07C
SMB_DATA_CPU — SMB_DATA 12,13,62,96
SMB_CLK_CPU — SMB_CLK 12,13,62,96

20150130 MV-1 Ita

3D3V_S0 — ED1801 LBAV99LT1G-1-GP 75.00099.O7D
12,13,62,96 SMB_DATA

3D3V_S0 — ED1802 LBAV99LT1G-1-GP 75.00099.O7D
12,13,62,96 SMB_CLK

3D3V_SUS

RN1803 — SRN2K2J-5-GP
SMB_CLK_CPU
SMB_DATA_CPU

RN1805 — SRN2K2J-5-GP
SML0_DATA_CPU
SML0_CLK_CPU

RN1806 — SRN2K2J-5-GP
PCH_KBC_CLK
PCH_KBC_DATA

CPU1G — 7 OF 19 — BROADWELL — LPC SMBUS SPI C-LINK

24,65,88 LPC_AD_CPU_P0 AU14 LAD0
24,65,88 LPC_AD_CPU_P1 AW12 LAD1
24,65,88 LPC_AD_CPU_P2 AY12 LAD2
24,65,88 LPC_AD_CPU_P3 AW11 LAD3
24,65,88 LPC_FRAME#_CPU AV12 LFRAME#

25 SPI_CLK_CPU AA3 SPI_CLK
25 SPI_CS_CPU_N0 Y7 SPI_CS0#
Y4 SPI_CS1#
AC2 SPI_CS2#
25 SPI_SI_CPU AA2 SPI_MOSI
25 SPI_SO_CPU AA4 SPI_MISO
25 SPI_WP_CPU Y6 SPI_IO2
25 SPI_HOLD_CPU AF1 SPI_IO3

SMBALERT#/GPIO11 AN2 MCP_GPIO11
SMBCLK AP2 SMB_CLK_CPU
SMBDATA AH1 SMB_DATA_CPU
SML0ALERT#/GPIO60 AL2 MCP_GPIO60
SML0CLK AN1 SML0_CLK_CPU
SML0DATA AK1 SML0_DATA_CPU
SML1ALERT#/PCHHOT#/GPIO73 AU4 MCP_GPIO73 20
SML1CLK/GPIO75 AU3 PCH_KBC_CLK 24,26,76
SML1DATA/GPIO74 AH3 PCH_KBC_DATA 24,26,76

CL_CLK AF2 CL_CLK1 58
CL_DATA AD2 CL_DATA1 58
CL_RST# AF4 CL_RST#1 58

BROADWELL-1-GP

DIMM1 / DIMM2 / Touchpad / XDP

EC / Thermal / GPU
EDP to LVDS / Sensor

3D3V_SUS — RN1804 SRN10KJ-6-GP
MCP_GPIO60
MCP_GPIO11
20 MCP_GPIO13
20 MCP_GPIO8

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCI-E/SMBUS/CLOCK/CL)
Size: A3 | Document Number: Laduree-BDW 15.6" | Rev: 1
Date: Thursday, February 12, 2015 | Sheet 18 of 102

SSID = CPU

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3 / PCIe* Port 6 Lane 0 SSD[1]	SATA 6Gb/s Port 2 / PCIe* Port 6 Lane 1 SSD[1]	SATA 6Gb/s Port 1 / PCIe* Port 6 Lane 2	SATA 6Gb/s Port 0 / PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD[1]	PCIe* Port 6 Lane 1 SSD[1]	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0

3D3V_RTC_AUX

R1928 1 — 20KR2F-L3-GP — 2
R1927 1 — 20KR2F-L3-GP — 2

20141203 SE - Ita

C1903 SC1U10V2KX-L1-GP

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

CPU1E — 5 OF 19 — BROADWELL

RTC Reset

C1904 SC1U10V2KX-L1-GP
G1901 GAP-OPEN

20141203 SE - Ita

R1904 1 — 1M1R2J-GP — 2
R1905 1 — 330KR2F-L-GP — 2

3D3V_RTC_AUX

CPU_XTAL_32K_X1 AW5
CPU_XTAL_32K_X2 AY5
SM_INTRUDER# AU6
PCH_INTVRMEN AV7
SRTC_RST# AV6
RTC_RST# AU7

RTCX1
RTCX2
INTRUDER#
INTVRMEN
SRTCRST#
RTCRST#

RTC

RN1902 SRN33J-5-GP-U

27 HDA_BITCLK_CODEC
27 HDA_RST#_CODEC
27 HDA_SDIN0_CPU
24 ME_UNLOCK
27 HDA_SDOUT_CODEC

HDA_BITCLK_CPU AW8
HDA_SYNC_CPU AV11
HDA_RST#_CPU AU8
AY10
AU12
AU11
AW10
AV10
AY8

HDA_BCLK/I2S0_SCLK
HDA_SYNC/I2S0_SFRM
HDA_RST#/I2S_MCLK
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_DOCK_EN#/I2S1_TXD
HDA_DOCK_RST#/I2S1_SFRM
I2S1_SCLK

AUDIO

R1908 1 — 1KR2J-L2-GP — 2
R1923 1 — 33R2J-L1-GP — 2

HDA_BITCLK_CODEC — FC1901 1 — SC4D7P50V2BN-GP — 2 — DY

Flash Descriptor Security Overide

HDA_SDOUT	Low = Default High = Enable

3D3V_SUS

2 — DY — 1 — R1902 1KR2J-L2-GP — 2 — HDA_SDOUT_CPU

4,96 XDP_TRST# AU62
96 PCH_JTAG_TCK AE62
96 PCH_JTAG_TDI AD61
96 PCH_JTAG_TDO AE61
96 PCH_JTAG_TMS AD62
AL11
AC4
96 PCH_JTAGX AE63
AV2

PCH_TRST#
PCH_TCK
PCH_TDI
PCH_TDO
PCH_TMS
RSVD#AL11
RSVD#AC4
JTAGX
RSVD#AV2

JTAG

BROADWELL-1-GP

20141012 SC - Terry

SATA_RN0/PERN6_L3 J5
SATA_RP0/PERP6_L3 H5
SATA_TN0/PETN6_L3 B15
SATA_TP0/PETP6_L3 A15

SATA_RX_CPU_N0 56
SATA_RX_CPU_P0 56
SATA_TX_CPU_N0 56
SATA_TX_CPU_P0 56

HDD

SATA_RN1/PERN6_L2 J8
SATA_RP1/PERP6_L2 H8
SATA_TN1/PETN6_L2 A17
SATA_TP1/PETP6_L2 B17

SATA_RX_CPU_N1 60
SATA_RX_CPU_P1 60
SATA_TX_CPU_N1 60
SATA_TX_CPU_P1 60

M2 SATA SSD

SATA_RN2/PERN6_L1 J6
SATA_RP2/PERP6_L1 H6
SATA_TN2/PETN6_L1 B14
SATA_TP2/PETP6_L1 C15

SATA_RN3/PERN6_L0 F5
SATA_RP3/PERP6_L0 E5
SATA_TN3/PETN6_L0 C17
SATA_TP3/PETP6_L0 D17

SATA

SATA0GP/GPIO34 V1 — SATA0GP_GPIO34
SATA1GP/GPIO35 U1 — SATA3GP_GPIO35
SATA2GP/GPIO36 V6 — SATA3GP_GPIO36
SATA3GP/GPIO37 AC1 — NMI_SMI_DBG# 20,24

SATA_IREF A12
RSVD#L11 L11
RSVD#K10 K10
SATA_RCOMP C12 — SATA_RCOMP — 3K01R2F-3-GP R1926 1 — 2 — 1D05V_VCCSATA3PLL_S0
SATALED# U3 — SATA_LED# 15,63

GP

20141012 SC - Terry

3D3V_S0
RN1901
SATA3GP_GPIO35 1
SATA0GP_GPIO34 2
3 4
SRN10KJ-L-GP

CPU_XTAL_32K_X1
R1901 1 — 10MR2J-L-GP — 2
CPU_XTAL_32K_X2

X1901
C1901 SC4P50V2CN-GP
C1902 SC4P50V2CN-GP
XTAL-32D768KHZ-67-GP

82.30001.G11

20141028_2 SC - Ita

3D3V_S0
R1929 1 — 10KR2J-L-GP — 2
SATA3GP_GPIO36
R1938 2 — 0R0402-PAD-1-GP — 1 — mSATA_DET# 60

20141103 SE - Ita

5V_S0
Q1901 2N7002KDW-GP
RTC_RST#_S
RTC_RST#
24 RTCRST_ON
HDA_SYNC_CPU
R1910 33R2J-L1-GP — 1 — HDA_SYNC_R
HDA_SYNC_CODEC 27
R1906 100KR2F-L3-GP
R1909 2KR2F-L1-GP

84.2N702.A3F
2nd = 75.00601.07C

UMA

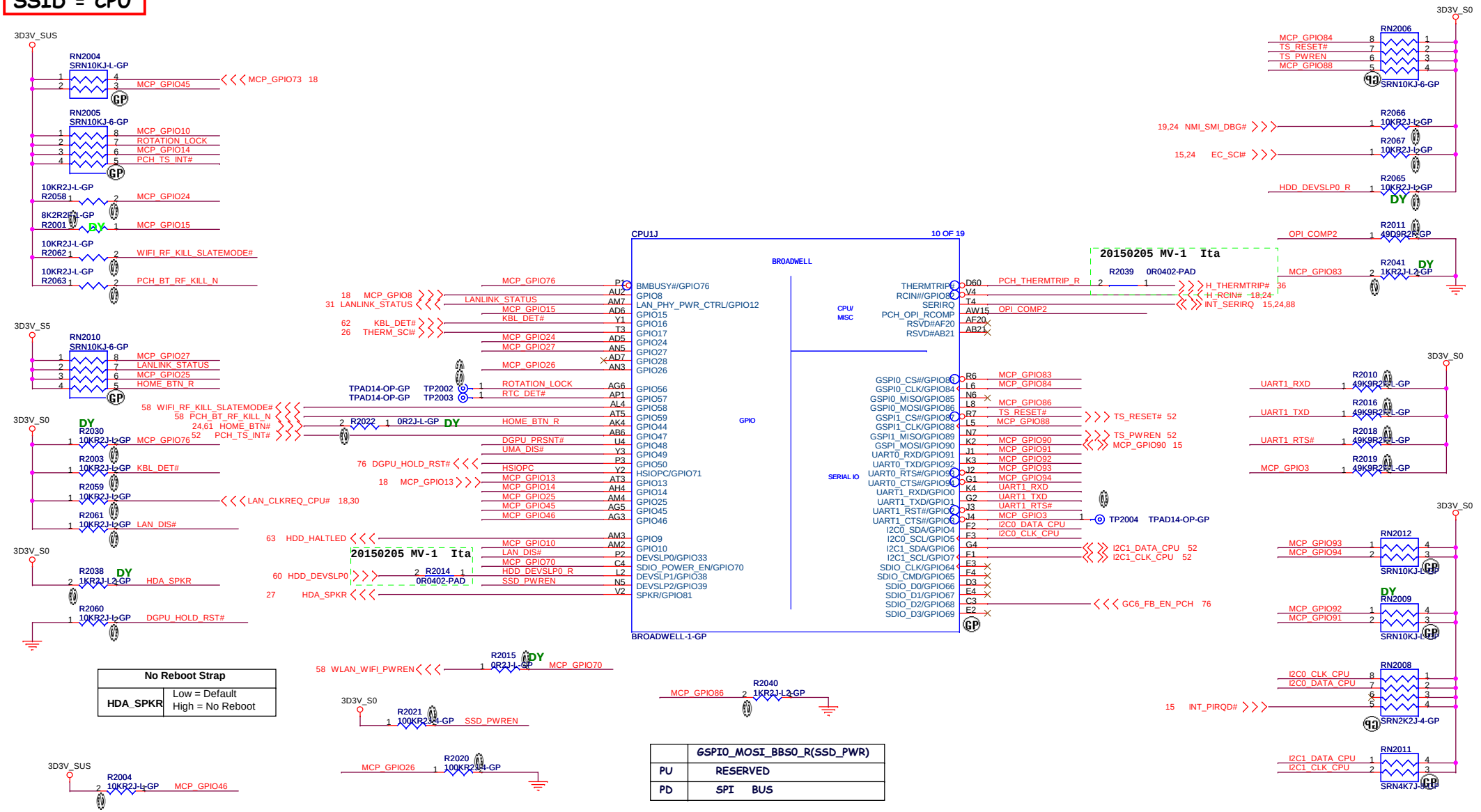
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RTC/LPC/SATA/HDA)

Size: A3 | Document Number: Laduree-BDW 15.6" | Rev: 1

Date: Thursday, February 12, 2015 | Sheet 19 of 102

SSID = CPU


CPU1J
10 OF 19
BROADWELL
BROADWELL-1-GP
GPIO
CPU MISC
SERIAL IO
BMBUSY#/GPIO76
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
GPIO16
GPIO17
GPIO24
GPIO27
GPIO28
GPIO26
GPIO56
GPIO57
GPIO58
GPIO59
GPIO44
GPIO47
GPIO48
GPIO49
GPIO50
HSIOPC/GPIO71
GPIO13
GPIO14
GPIO25
GPIO45
GPIO46
GPIO9
GPIO10
DEVSLP0/GPIO33
SDIO_POWER_EN/GPIO70
DEVSLP1/GPIO38
DEVSLP2/GPIO39
SPKR/GPIO81
THERMTRIP#
RCIN#/GPIO80
SERIRQ
PCH_OPI_RCOMP
RSVD#AF20
RSVD#AB21
GSPI0_CS#/GPIO83
GSPI0_CLK/GPIO84
GSPI0_MISO/GPIO85
GSPI0_MOSI/GPIO86
GSPI1_CS#/GPIO87
GSPI1_CLK/GPIO88
GSPI1_MISO/GPIO89
GSPI_MOSI/GPIO90
UART0_RXD/GPIO91
UART0_TXD/GPIO92
UART0_RTS#/GPIO93
UART0_CTS#/GPIO94
UART1_RXD/GPIO0
UART1_TXD/GPIO1
UART1_RST#/GPIO2
UART1_CTS#/GPIO3
I2C0_SDA/GPIO4
I2C0_SCL/GPIO5
I2C1_SDA/GPIO6
I2C1_SCL/GPIO7
SDIO_CLK/GPIO64
SDIO_CMD/GPIO65
SDIO_D0/GPIO66
SDIO_D1/GPIO67
SDIO_D2/GPIO68
SDIO_D3/GPIO69
20150205 MV-1 Ita
20150205 MV-1 Ita
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
GSPI0_MOSI_BBS0_R(SSD_PWR)
PU RESERVED
PD SPI BUS
UMA
PX
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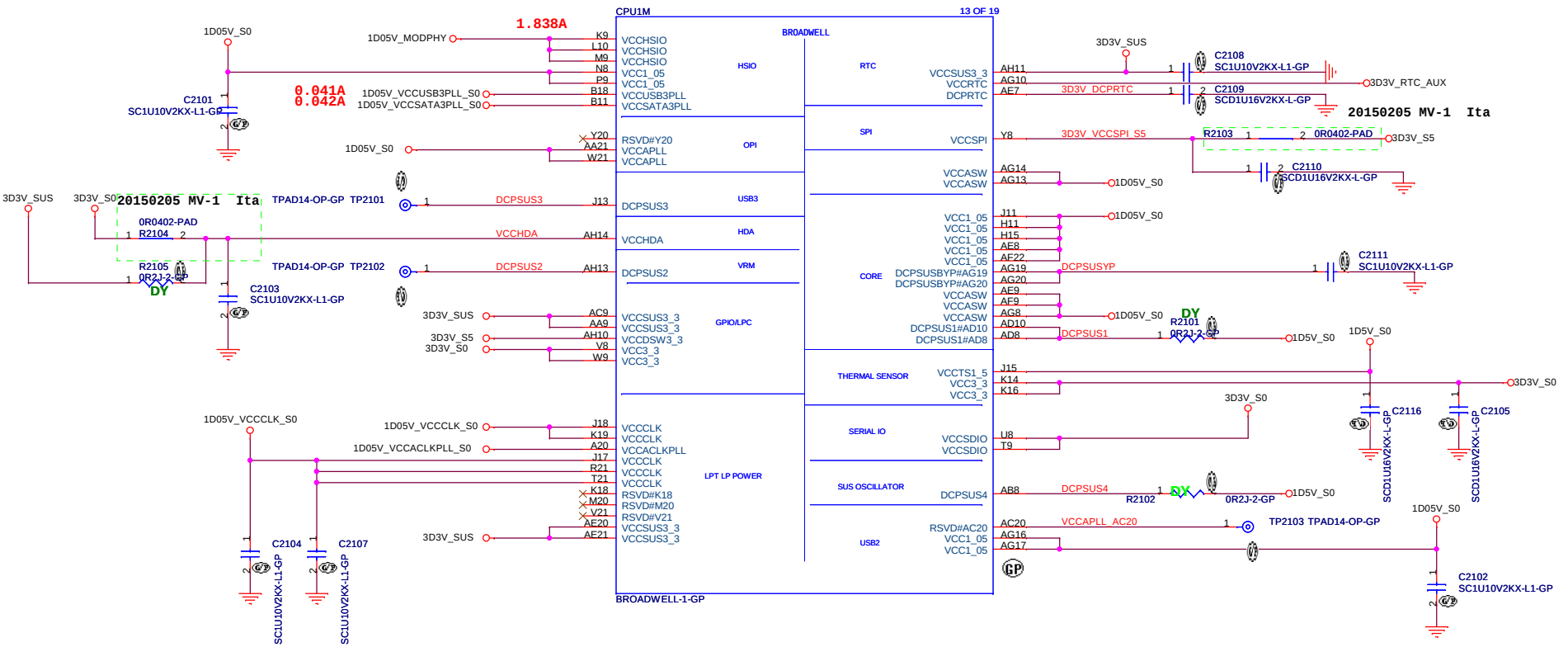
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (GPIO/MISC)
Size A3
Document Number
Laduree-BDW 15.6"
Rev 1
Date: Thursday, February 12, 2015
Sheet 20 of 102

SSID = CPU

Notes:

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



UMA

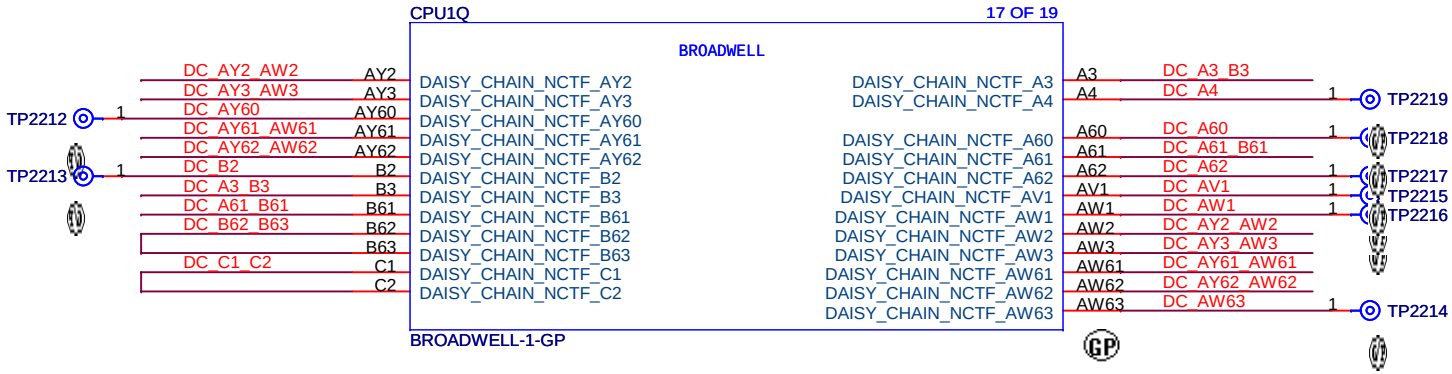
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

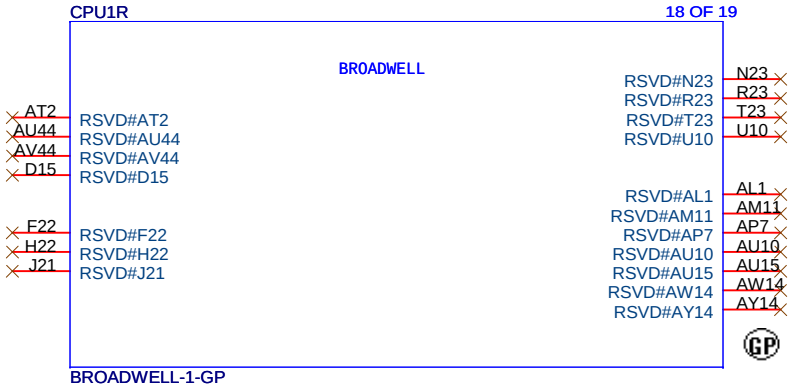
Title: **CPU (POWER1)**

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Friday, February 06, 2015 Sheet 21 of 102

SSID = CPU





UMA

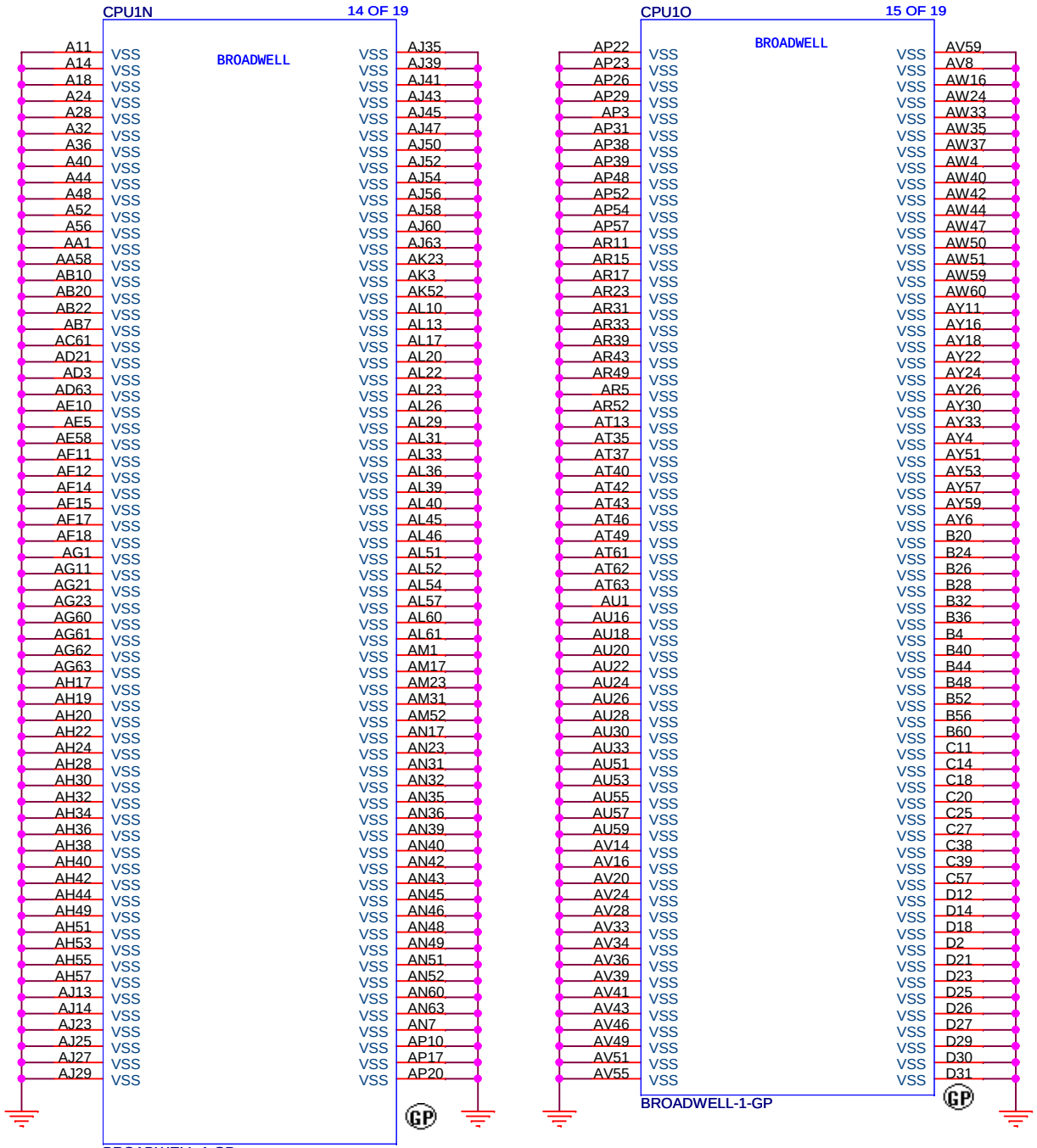
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (RSVD)*

Size	Document Number	Rev
A4	Laduree-BDW 15.6"	1

Date: Friday, January 30, 2015 Sheet 22 of 102

SSID = CPU



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VSS)**

Size	Document Number	Rev
A4	Laduree-BDW 15.6"	1

Date: Friday, January 30, 2015 Sheet 23 of 102

SSID = KBC

KBC9028Q

U2401

KB9028Q-C-GP

071.09028.000G

For EC power consumption reserver

20150205 MV-1 Ita

20150204 MV-1 Ita

CONFIRM EC THIS PIN PM_PWRBTN# PIN HI OUPUT

S0_PWR_GOOD ==DELAY 99ms

PCB VERSION

-1

PCB VERSION ADC(PIR98)		Pull-Low Register	Pull-High Register	Typical Voltage
SA		100.0 K	10.0 K	3.000 V
SB		100.0 K	20.0 K	2.750 V
SC		100.0 K	33.0 K	2.481 V
SD		100.0 K	47.0 K	2.245 V
-1	SE	100.0 K	64.9 K	2.001 V
-2	-1	100.0 K	76.8 K	1.867 V
-3	-2	100.0 K	100.0 K	1.650 V
-4	-3	100.0 K	143.0 K	1.358 V
-5	-4	100.0 K	174.0 K	1.204 V

MODEL ID

		Pull-Low Register	Pull-High Register	Typical Voltage
HEVIN	BDW-Y	100.0 K	10.0 K	3.000 V
	SKL-Y	100.0 K	20.0 K	2.750 V
	BSW	100.0 K	33.0 K	2.481 V
Fauchon	BDW-U	100.0 K	47.0 K	2.245 V
	SKL-U	100.0 K	64.9 K	2.001 V
Bonie	CZL	100.0 K	76.8 K	1.867 V
Laduree	BDW-U	100.0 K	100.0 K	1.650 V
	SKL-U	100.0 K	143.0 K	1.358 V
		100.0 K	174.0 K	1.204 V

ene 20140326

ENE EDI

HP Limit Signal Detect

83.00099.U11

68.00084.921

83.00355.F1F

Title	KBC_NPCE285PA0DX-GP
Size / Document Number	Laduree-BDW 15.6"
Rev	1
Date	Thursday, February 12, 2015
Sheet	24 of 102

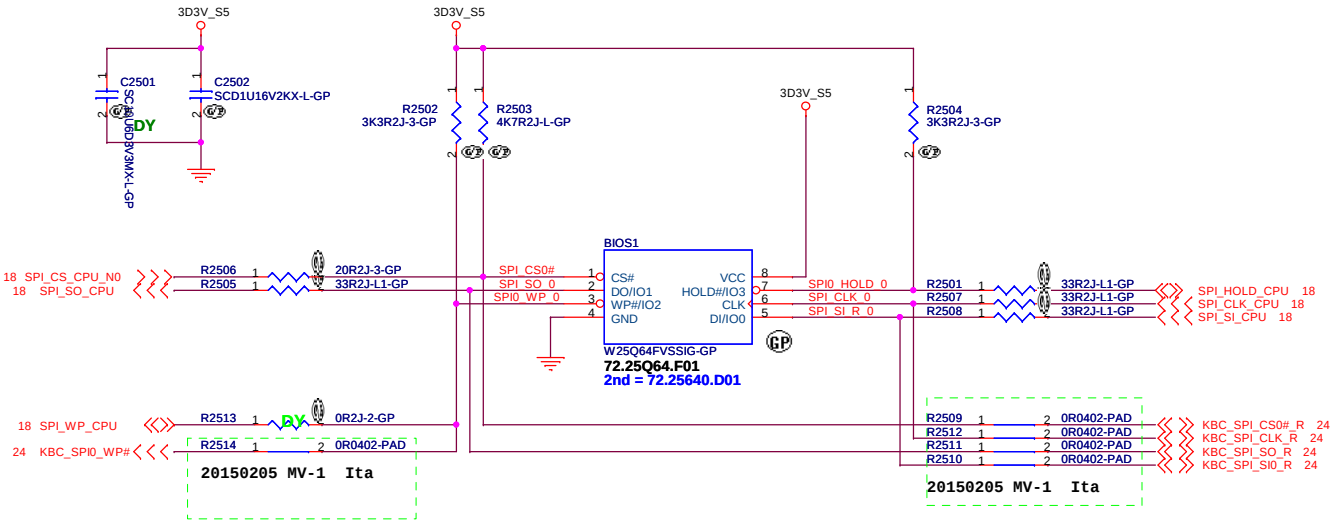
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

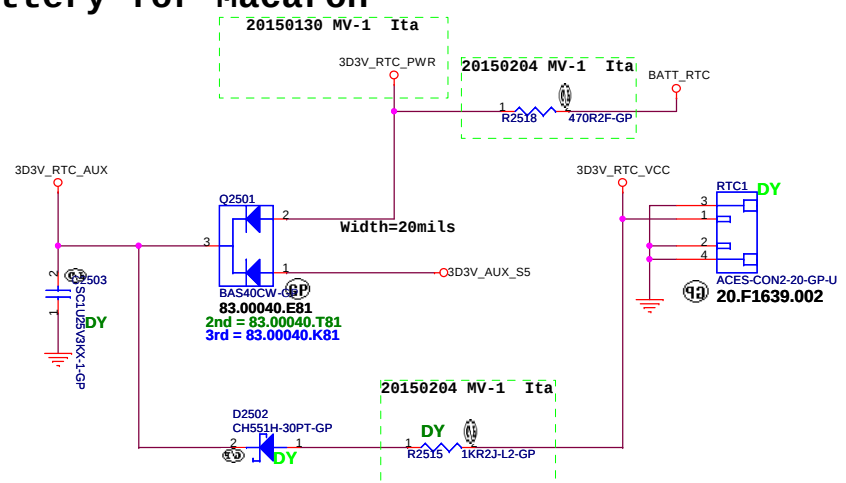
SPI ROM Equal length need to less than 500mil

20150213 MV-1 Ita



Vinafix

SSID = RBAT **No RTC battery for Macaron**



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

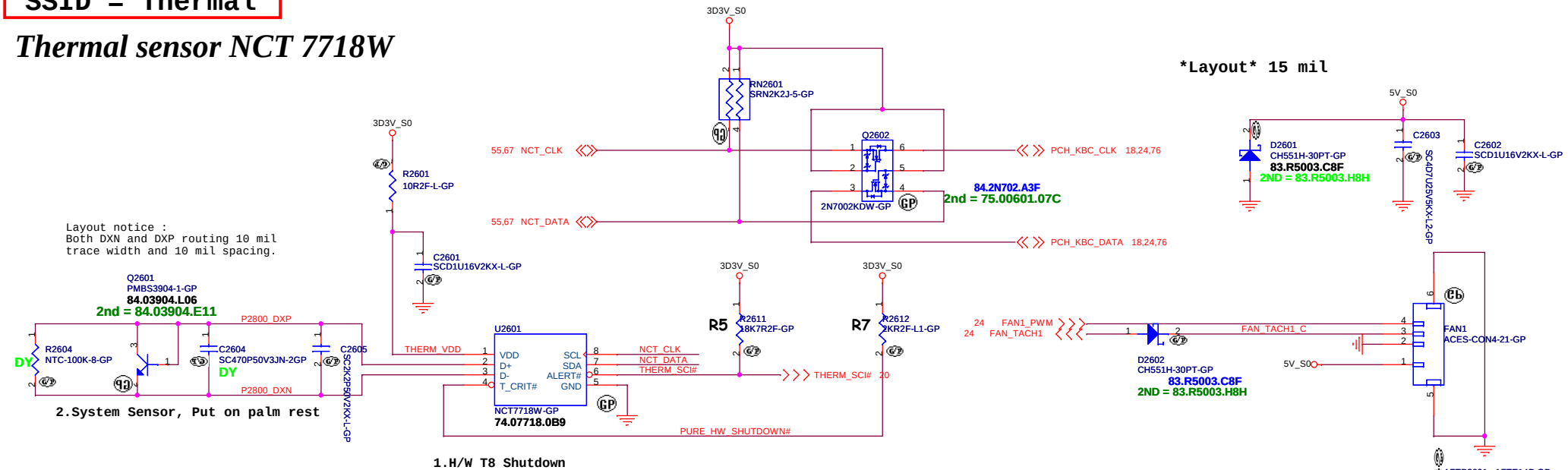
Title: ***Flash(KBC+PCH)/RTC***

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Friday, February 13, 2015 Sheet 25 of 102

SSID = Thermal

Thermal sensor NCT 7718W



NCT7718W I2C/ SMBusTM address is 1001100xb (x is R/W bit).

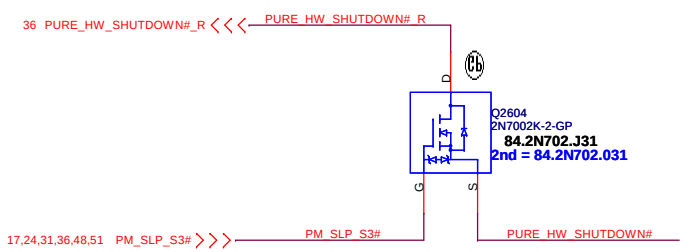
98 / 4C

ALERT# /T CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

T8=85 degree



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G788P81/Fan Controllor P2793***

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 26 of 102

Vout = 4.75 V

AUDIO CODEC ALC3227

20150205 MV-1 Ita

U2701

ALC3227-CG-GP
071.03227.0003

Port Arrangement

- Port A---> x
- Port B---> x
- Port C---> x
- Port D---> Speaker
- Port E---> x
- Port F---> Mic In
- Port G---> x
- Port H---> x
- Port I---> Head Phone

Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

Digital GND & AUD_AGND

Tie Analog GND and Digital GND under codec by a single point

audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP

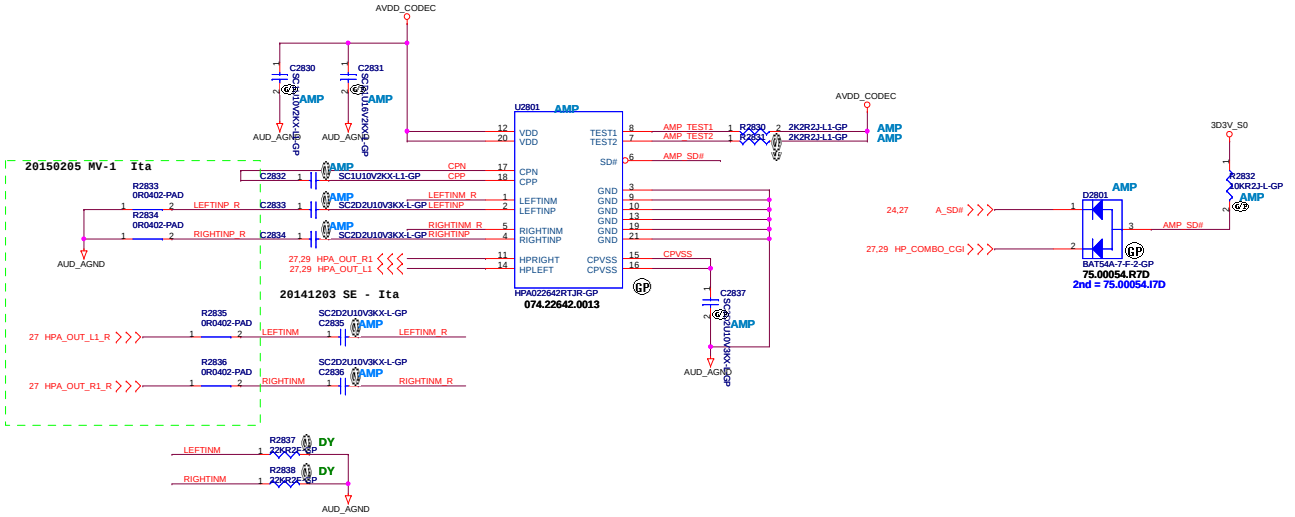
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec_ALC3225

Size: Custom | Document Number: Laduree-BDW 15.6" | Rev: 1

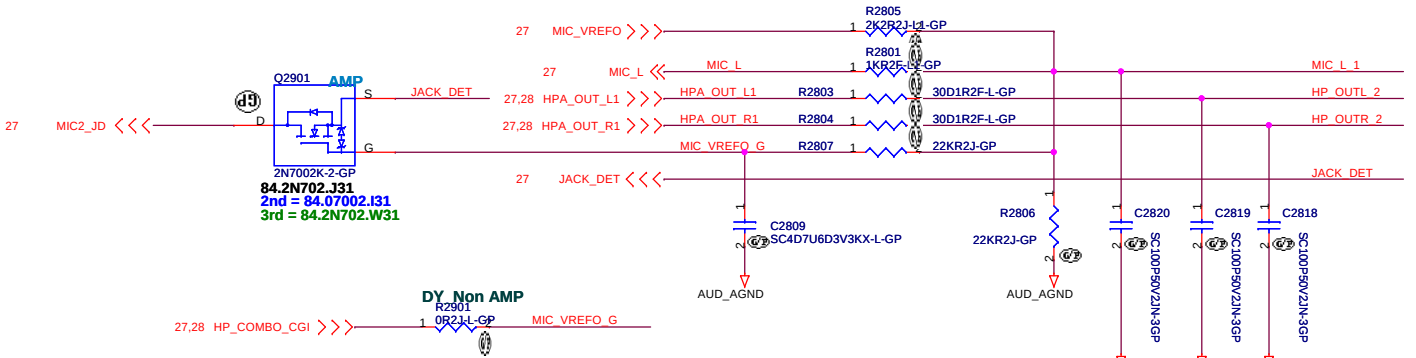
Date: Thursday, February 12, 2015 | Sheet 27 of 102

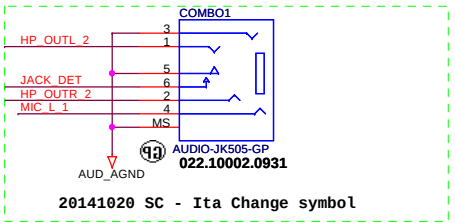


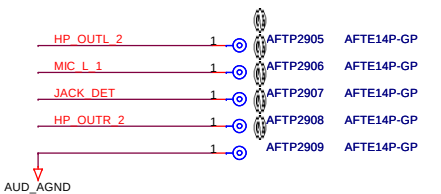
UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Audio AMP_HPA0022642RTJR	
Size: Custom	Document Number: Laduree-BDW 15.6"	Rev: 1
Date: Thursday, February 12, 2015	Sheet 28 of 102	

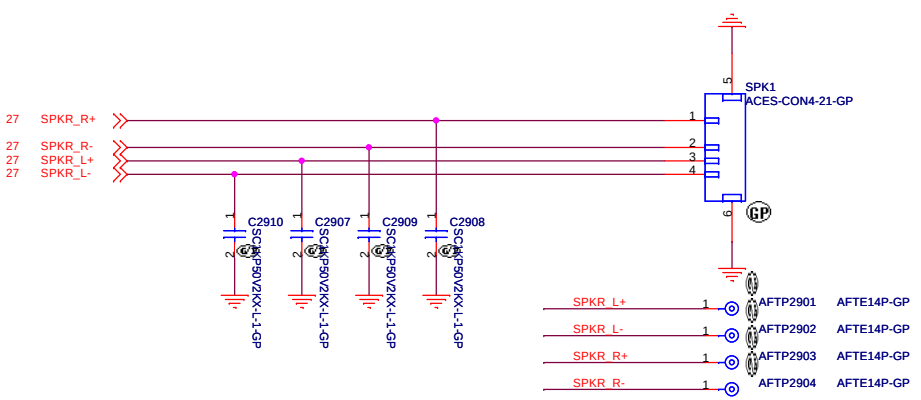
Combo-Jack (Headphone & MIC)







Speaker



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Audio Combo Jack / SPK Conn***	
Size A3	Document Number **Laduree-BDW 15.6"**	Rev **1**
Date: Thursday, February 12, 2015	Sheet 29 of 102	

EEPROM LED OPTION USE '00'
=> LED0 : ACT (Amber)
=> LED1 : LINK (White)
(BOTH 10/100 & GIGA CHIP)
(Power down => Kept high)

Layout:
For RTL8111G(S)
* Place C3021 to C3024 close to each VDD10 pin--3, 8,

C3032: colse to Pin8
C3025 close to Pin30
C3026: close to Pin3
C3031: close to Pin22

20140802

L3001 IND-2D2UH297-GP
REGOUT
1V_LAN_VDD10
68.2R21G.10P
C3003 SCD1U16V3KX-L-GP
C3027 SCD1U16V2KX-L-GP
C3025 SCD1U16V2KX-L-GP
C3026 SCD1U16V2KX-L-GP
C3031 SCD1U16V2KX-L-GP
C3032 SCD1U16V2KX-L-GP
C3024 SCD1U16V2KX-L-GP
C3030 SC1U10V2KX-L-GP
C3024 / C3030 close to Pin22

40 mils
C3008: close to Pin32
C3007: close to Pin11 (RTL8111 only)
C3009 and C3011 close pin23

3D3V_S5
R3004 0R0603-PAD-1-GP-U
3D3V_LAN_VDD33
20150210 MV-1 Ita
C3009 SCD1U16V3KX-L-GP DY
C3010 SCD1U16V3KX-L-GP DY
C3007 SCD1U16V2KX-L-GP
C3008 SCD1U16V2KX-L-GP
C3011 SCD1U16V2KX-L-GP
C3012 SCD1U16V3KX-L-GP
C3011 / C3012 close to Pin23

RSET
R3008 2K49R2F-2-L-GP

U3001
3D3V_LAN_VDD33
1V_LAN_VDD10
AVDD10 3
AVDD10 8
AVDD10 30
AVDD33 32
AVDD33 11
VDDREG 23
DVDD10 22
MDIP0 1
MDIN0 2
MDIP1 4
MDIN1 5
MDIP2 6
MDIN2 7
MDIP3 9
MDIN3 10
LANWAKE# 21
ISOLATE# 20
HSIP 13
HSIN 14
HSOP 17
HSON 18
PERST# 19
CLKREQ# 12
REFCLK_P 15
REFCLK_N 16
CKXTAL1 28
CKXTAL2 29
LED0 27
LED1/GPO 26
LED2 25
REGOUT 24
RSET 31
GND 33
PCIE_TX_LAN_P3 16
PCIE_TX_LAN_N3 16
PCIE_RX_LAN_P3
PCIE_RX_LAN_N3
SCD1U16V2KX-L-GP
C3028
C3029
PCIE_RX_CPU_P3 16
PCIE_RX_CPU_N3 16
PLT_RST# 17,24,30,38,63,65,76,88,96
LAN_CLKREQ_CPU# 18,20
LAN_CLK_CPU 18
LAN_CLK_CPU# 18
LAN_XTAL_25M_IN
LAN_XTAL_25M_OUT
AMBER_LED# 31
WHITE_LED# 31
LAN_LED3#
TP3001 TPAD14-OP-GP
REGOUT
RSET
PCIE_WAKE# LAN
ISOLATEB
RTL8111HSH-CG-GP
071.8111H.M002

3D3V_S0
R3010 1KR2J-L2-GP
ISOLATEB
R3013 15K4R2F-GP

C3022 SC12P50V2JN-3GP
X3001
LAN_XTAL_25M_IN
DY R3009 1MR2J-L3-GP
LAN_XTAL_25M_OUT
C3023 SC15P50V2JN-L-GP
XTAL-25MHZ-181-GP
82.30020.G71
2nd = 82.30020.G61

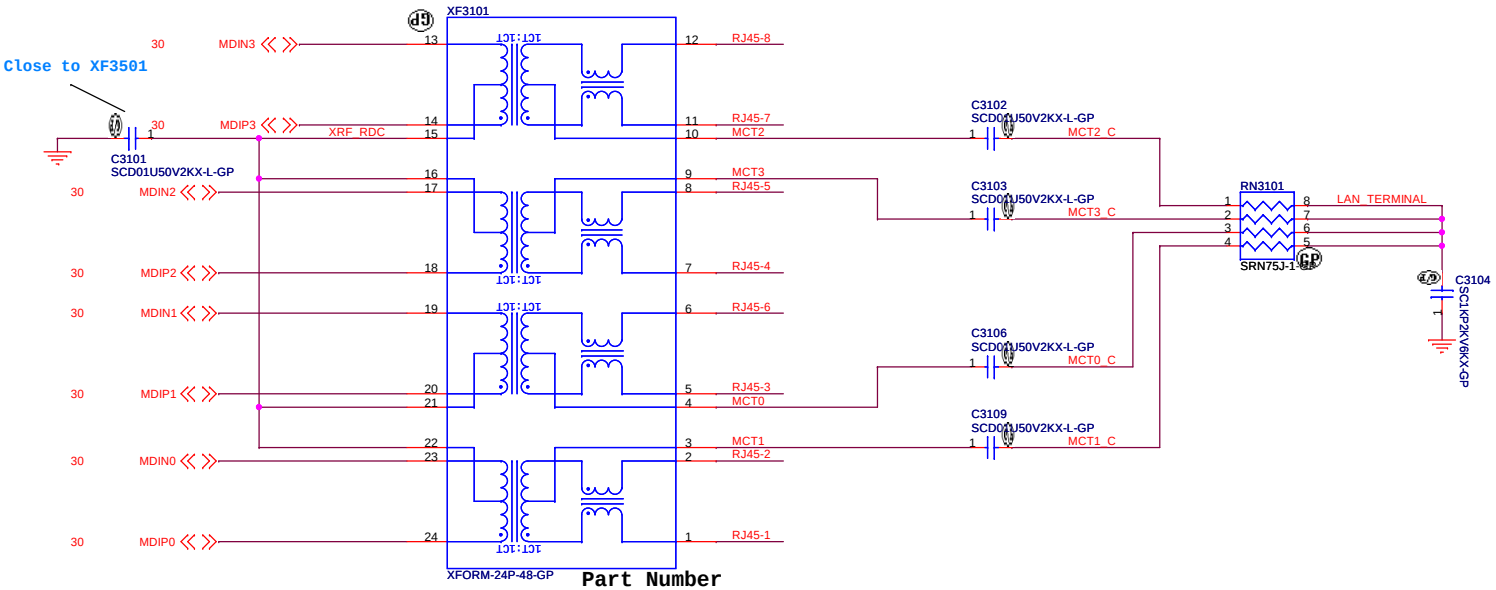
3D3V_S5
R3006 4K02R2F-GP
PCIE_WAKE# 17,24,58,63
PCIE_WAKE#_LAN_B
Q3002 LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.03904.X11
3rd = 84.03904.E11
0822-Anthony
R3012 2KR2J-1-GP
R3011 0R2J-2-GP
DY
PCIE_WAKE#_LAN

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

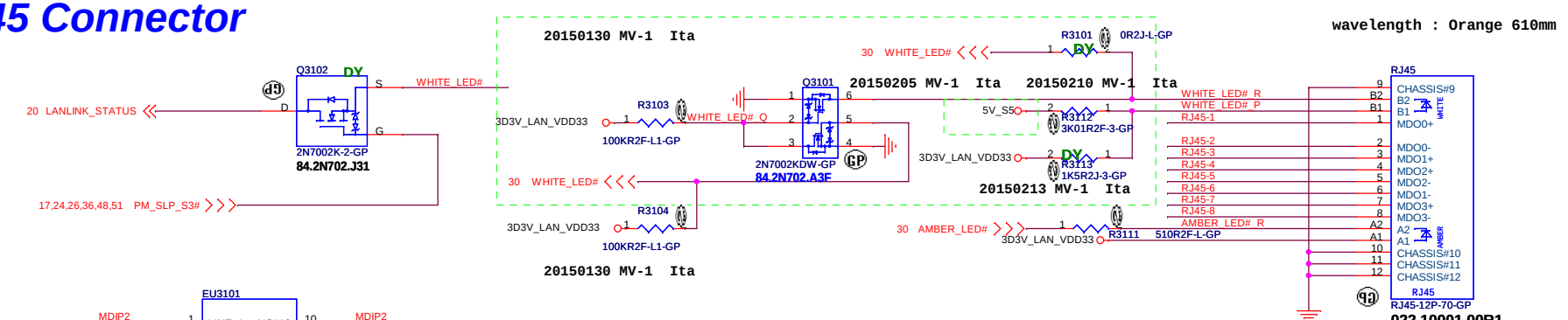
Title: LAN(RTL8411)
Size: Custom
Document Number: Laduree-BDW 15.6"
Rev: 1
Date: Thursday, February 12, 2015
Sheet 30 of 102

White LED for connectivity and Amber LED for activity located on RJ-45 connector

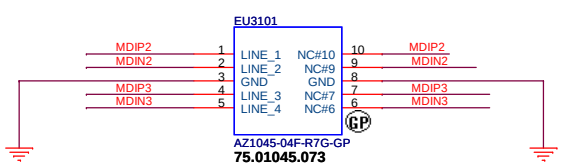


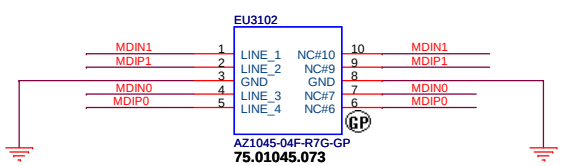
Part Number
Main:68.69241.301
2nd:68.IH080.301

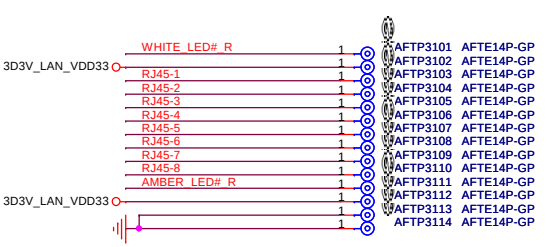
RJ45 Connector



wavelength : Orange 610mm







Green
10(+),9(-)

YELLOW
12(+),13(-)

(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat, except RJ-45 moat.

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (LAN+VGA) CONNECTOR

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Friday, February 13, 2015 Sheet 31 of 102

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RTS5237(CARD READER)

Size	Document Number	Rev
A3	**Laduree-BDW 15.6"**	1

Date: Friday, January 30, 2015 Sheet 32 of 102

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
A3	**Laduree-BDW 15.6"**	1

Date: Friday, January 30, 2015 Sheet 33 of 102

USB3.0 Charger Port

20150205 MV-1 Ita

16 USB30_RX_CPU_N1 — R3401 — 0R0402-PAD — USB3_RX1-
16 USB30_RX_CPU_P1 — R3402 — 0R0402-PAD — USB3_RX1+

35 USB_CHAR_PN0 — TR3402 — USB2_0-
35 USB_CHAR_PP0 — FILTER-4P-6-GP — USB2_0+

16 USB30_TX_CPU_N1 — C3401 SCD1U16V2KX-L-GP — USB3_TX1- C — R3405 — 0R0402-PAD — USB3_TX1-
16 USB30_TX_CPU_P1 — C3402 SCD1U16V2KX-L-GP — USB3_TX1+ C — R3406 — 0R0402-PAD — USB3_TX1+

USB_VCCA — USB31
USB2_0- / USB2_0+ — D- / D+
USB3_RX1- / USB3_RX1+ — SSRX- / SSRX+
USB3_TX1- / USB3_TX1+ — SSTX- / SSTX+
VBUS, CHASSIS#10, CHASSIS#11, CHASSIS#12, CHASSIS#13, PGND, GND
USB3.0
SKT-USB13-211-GP
022.10005.00U1

USB_VCCA — AFTP3401 AFTE14P-GP
USB_VCCA — AFTP3402 AFTE14P-GP
USB2_0- — AFTP3403 AFTE14P-GP
USB2_0+ — AFTP3404 AFTE14P-GP
USB3_TX1- — AFTP3405 AFTE14P-GP
USB3_TX1+ — AFTP3406 AFTE14P-GP
USB3_RX1- — AFTP3407 AFTE14P-GP
USB3_RX1+ — AFTP3408 AFTE14P-GP
AFTP3409 AFTE14P-GP
AFTP3410 AFTE14P-GP

USB2_0+ — C3405 — DY — SC5D6P50V2CN-1GP
USB2_0- — C3406 — DY — SC5D6P50V2CN-1GP

ED3401 — DY
USB2_0- — I/O1 — I/O4 — USB2_0+
GND — VDD — USB_VCCA
I/O2 — I/O3
AZC099-04S-1-GP
75.09904.07C

ED3402 — DY
USB2_1- — I/O1 — I/O4 — USB2_1+
GND — VDD — USB_VCCB
I/O2 — I/O3
AZC099-04S-1-GP
75.09904.07C

EU3401 — DY
USB3_TX1+ / USB3_TX1- — LINE_1 / LINE_2 — NC#10 / NC#9 — USB3_TX1+ / USB3_TX1-
GND — LINE_3 — GND / NC#7 — USB3_RX1+ / USB3_RX1-
USB3_RX1+ / USB3_RX1- — LINE_4 — NC#6
AZ1045-04F-R7G-GP
75.01045.073

EU3402 — DY
USB3_TX2+ / USB3_TX2- — LINE_1 / LINE_2 — NC#10 / NC#9 — USB3_TX2+ / USB3_TX2-
GND — LINE_3 — GND / NC#7 — USB3_RX2+ / USB3_RX2-
USB3_RX2+ / USB3_RX2- — LINE_4 — NC#6
AZ1045-04F-R7G-GP
75.01045.073

USB3.0 Port

20150205 MV-1 Ita

16 USB30_RX_CPU_N2 — R3407 — 0R0402-PAD — USB3_RX2-
16 USB30_RX_CPU_P2 — R3412 — 0R0402-PAD — USB3_RX2+

16 USB_CPU_PN1 — TR3404 — USB2_1-
16 USB_CPU_PP1 — FILTER-4P-6-GP — USB2_1+

16 USB30_TX_CPU_N2 — C3404 SCD1U16V2KX-L-GP — USB3_TX2- C — R3408 — 0R0402-PAD — USB3_TX2-
16 USB30_TX_CPU_P2 — C3403 SCD1U16V2KX-L-GP — USB3_TX2+ C — R3409 — 0R0402-PAD — USB3_TX2+

USB_VCCB — USB32
USB2_1- / USB2_1+ — D- / D+
USB3_RX2- / USB3_RX2+ — SSRX- / SSRX+
USB3_TX2- / USB3_TX2+ — SSTX- / SSTX+
VBUS, CHASSIS#10, CHASSIS#11, CHASSIS#12, CHASSIS#13, PGND, GND
USB3.0
SKT-USB13-211-GP
022.10005.00U1

USB_VCCB — AFTP3413 AFTE14P-GP
USB_VCCB — AFTP3414 AFTE14P-GP
USB2_1- — AFTP3415 AFTE14P-GP
USB2_1+ — AFTP3416 AFTE14P-GP
USB3_TX2- — AFTP3417 AFTE14P-GP
USB3_TX2+ — AFTP3418 AFTE14P-GP
USB3_RX2- — AFTP3419 AFTE14P-GP
USB3_RX2+ — AFTP3420 AFTE14P-GP
AFTP3411 AFTE14P-GP
AFTP3412 AFTE14P-GP

USB2_1+ — C3407 — DY — SC5D6P50V2CN-1GP
USB2_1- — C3408 — DY — SC5D6P50V2CN-1GP

5V_S5 — U3403
GND, IN, IN, EN# — NC#8, OUT, OUT, FLG#
AP2501M8-13-GP
074.02501.0079

FC3421 SCD1U16V2KX-L-GP — RF
C3410 SCD1U16V2KX-L-GP
24,63 USB_PWR_EN#

5V_S5 — R3413 0R2J-2-GP — DY — U3403_5
20141211 SE - Ita

100 mils

USB_VCCB — C3420 SCD1U16V2KX-L-GP
C3415 SCD1U16V2KX-L-GP
C3409 SC10P50V2JN-4GP
C3412 SC22U6D3V5MXL3-GP
C3411 SC47U6D3V5MX-1-GP
C3413 SC47U6D3V5MX-1-GP
USB_VCCB — FC3410 SCD1U25V2KX-L-GP — RF
FC3411 SCD1U25V2KX-L-GP — DY

USB3_RX1- — FC3401 — SC6D8P50V2CN-GP — DY
USB3_RX1+ — FC3402 — SC6D8P50V2CN-GP — DY
USB3_TX1- — FC3403 — SC6D8P50V2CN-GP — DY
USB3_TX1+ — FC3404 — SC6D8P50V2CN-GP — DY
USB3_RX2- — FC3405 — SC6D8P50V2CN-GP — DY
USB3_TX2- — FC3406 — SC6D8P50V2CN-GP — DY
USB3_RX2+ — FC3407 — SC6D8P50V2CN-GP — DY
USB3_TX2+ — FC3408 — SC6D8P50V2CN-GP — DY

USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

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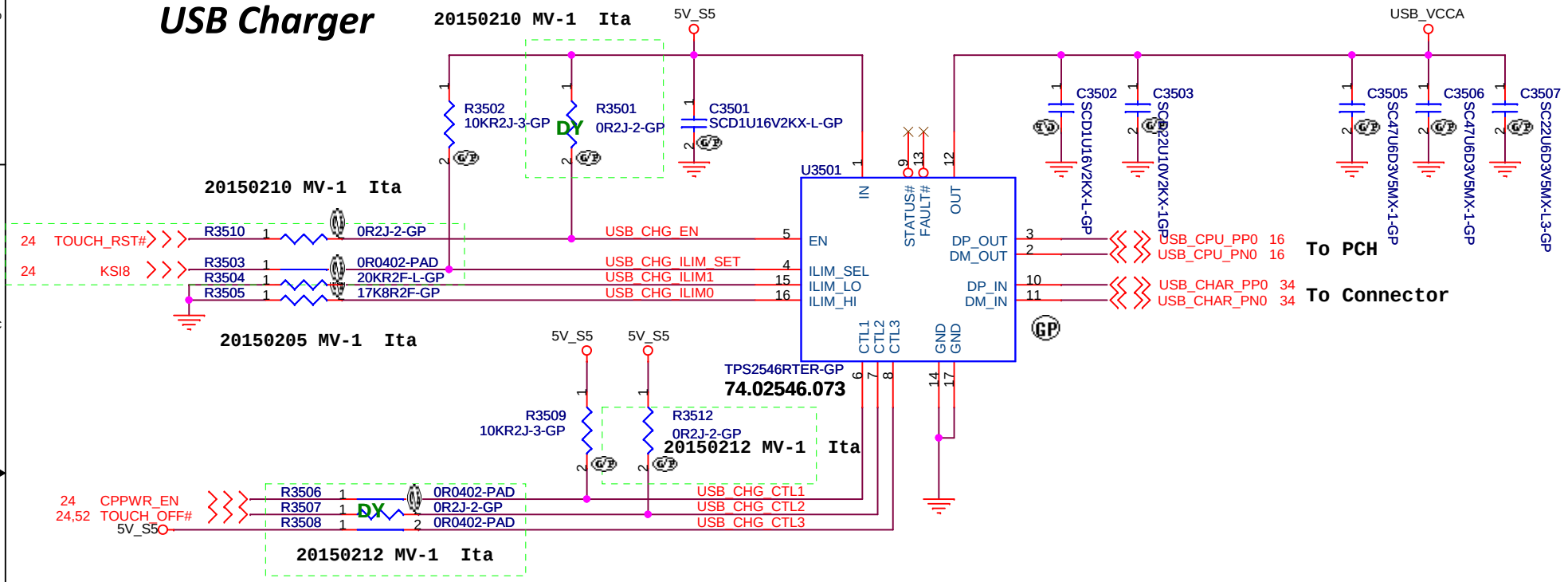
Title: USB 3.0 Port

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 34 of 102

USB Charger



UMA

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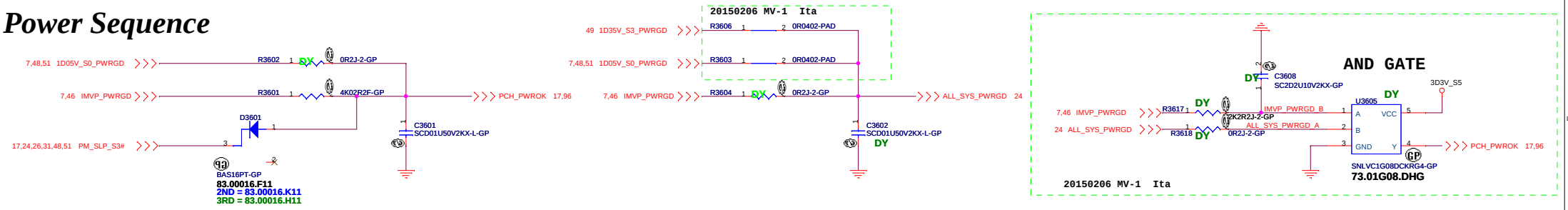
Title: USB CHARGER

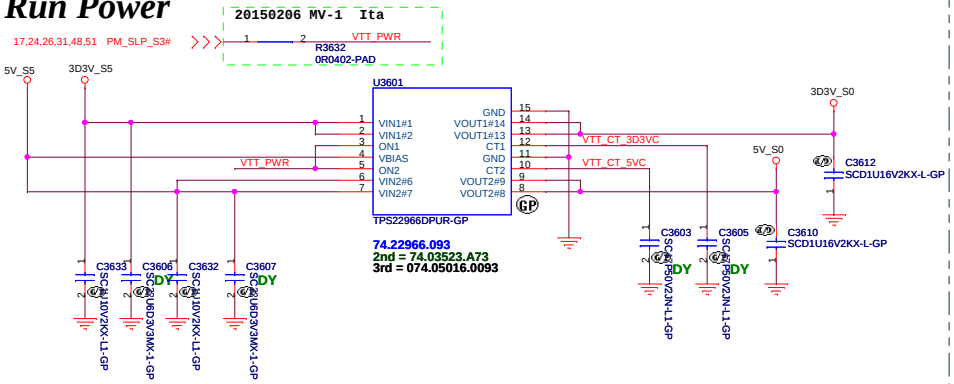
Size	Document Number	Rev
A4	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 35 of 102

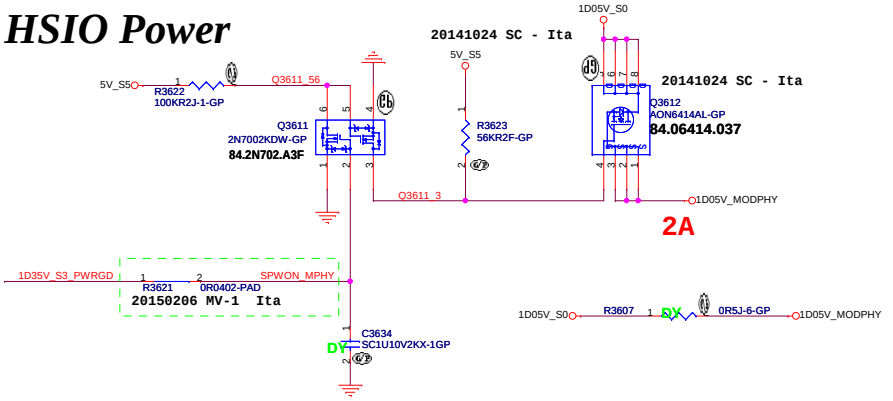
Power Sequence



Run Power

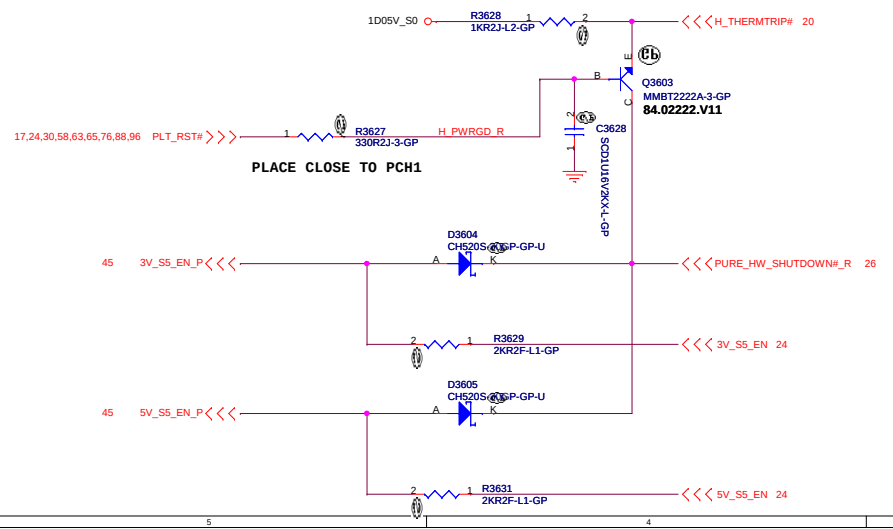


HSIO Power

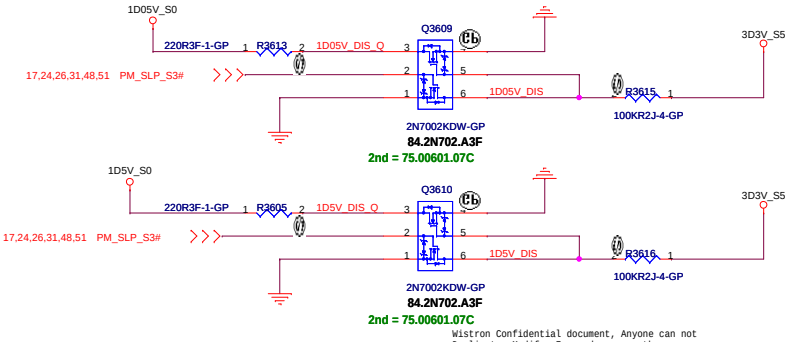


To 3V/ 5V Power IC S5 ENABLE

2014.03.18
DESIGN GUIDE 602 Boardwell pop



Discharge circuit



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Title: Power Plane Enable & SEQUENCE

Size: Custom | Document Number: Laduree-BDW 15.6" | Rev: 1

Date: Thursday, February 12, 2015 | Sheet 36 of 102

UMA

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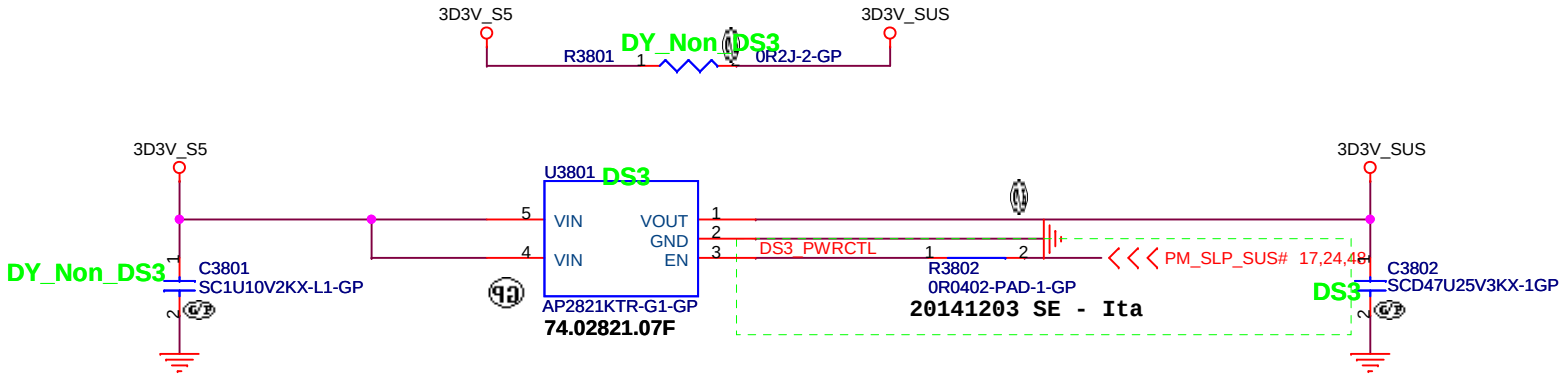
Title

ADAPTER OCP / S3 reduction

Size	Document Number	Rev
A4	Laduree-BDW 15.6"	1

Date: Friday, January 30, 2015 Sheet 37 of 102



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Title

DS3

Size	Document Number	Rev
A4	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 38 of 102

Power Sequence

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Title: ***1D05_M***

Size	Document Number	Rev
A3	**Laduree-BDW 15.6"**	1

Date: Friday, January 30, 2015 Sheet 39 of 102

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Title

Connected Standby1

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

Date: Friday, January 30, 2015 Sheet 40 of 102

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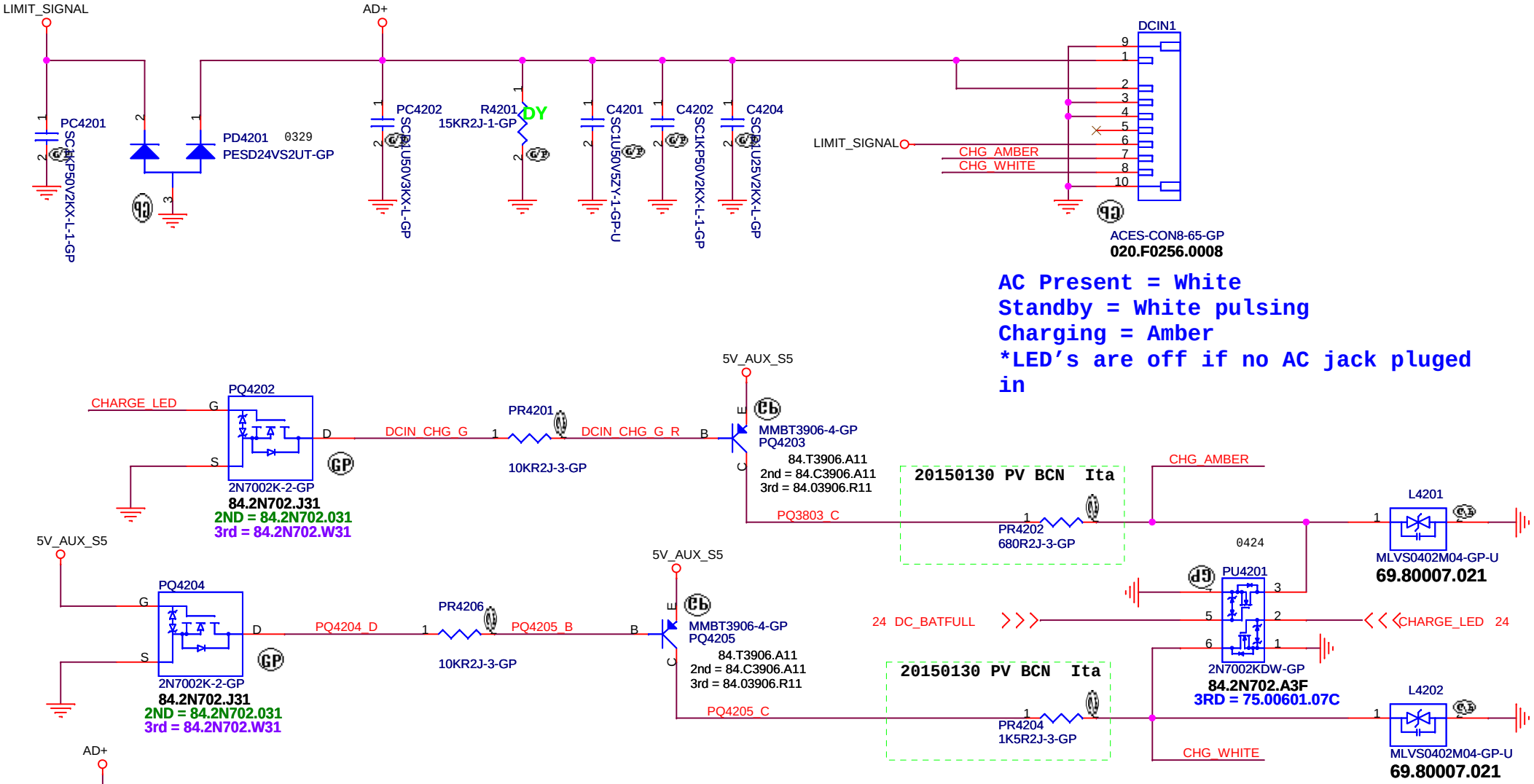
Title

Connected Standby2

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

Date: Friday, January 30, 2015 Sheet 41 of 102



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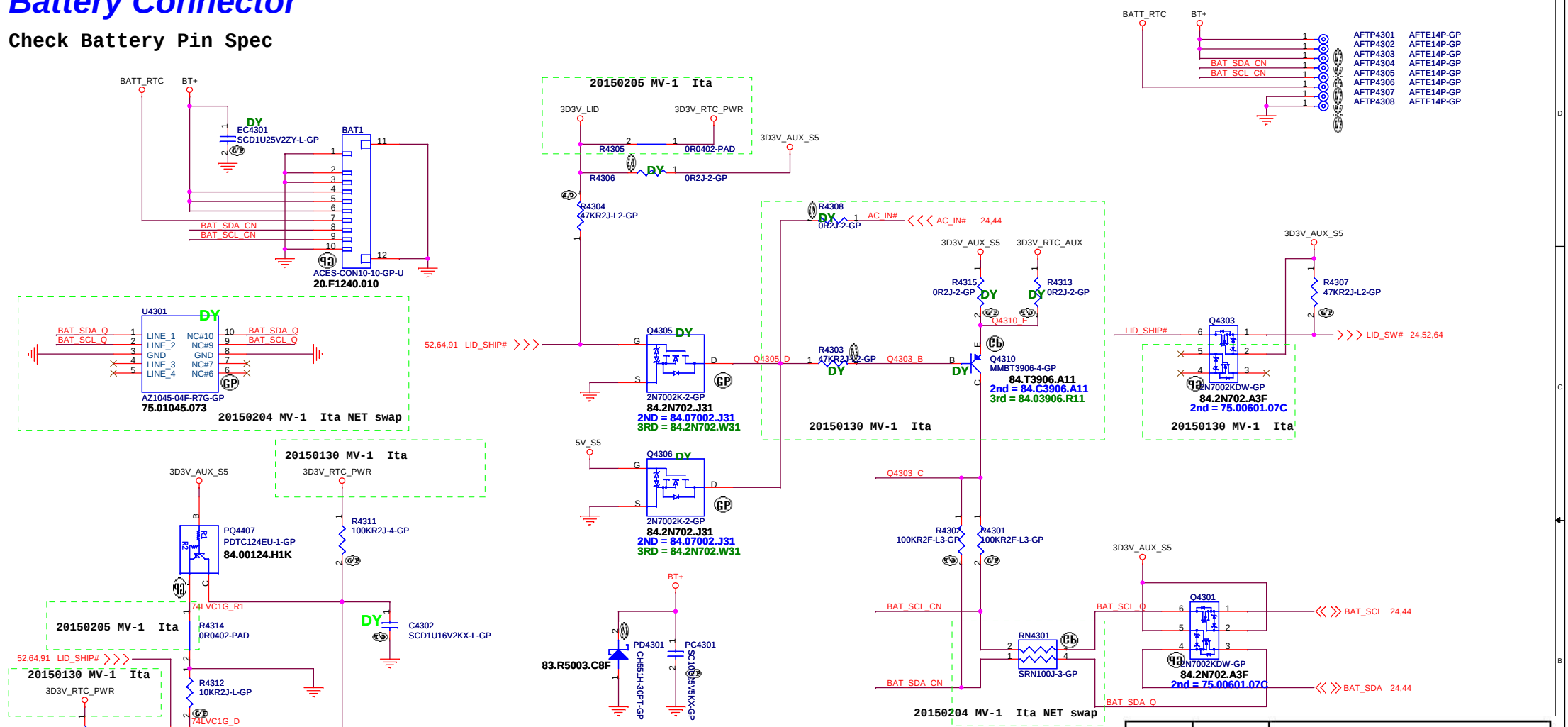
Title: **DCIN JACK**

Size	Document Number	Rev
A4	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 42 of 102

Battery Connector

Check Battery Pin Spec



Pin No.	Symbol	Comments
1,2	GND	Batt-, Battery Negative Terminal
3	B/I	Connected to GND.
4,5,6	BATT+	Batt+, Battery Positive Terminal.
7	RTC	
8	SMD	SMBus data interface I/O pin.
9	SMC	SMBus clock interface I/O pin
10	GND	Batt-, Battery Negative Terminal

Table 4. Function table for asynchronous operation[1]

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L

Table 5. Function table for synchronous operation[1]

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size: A3 | Document Number: Laduree-BDW 15.6" | Rev: 1

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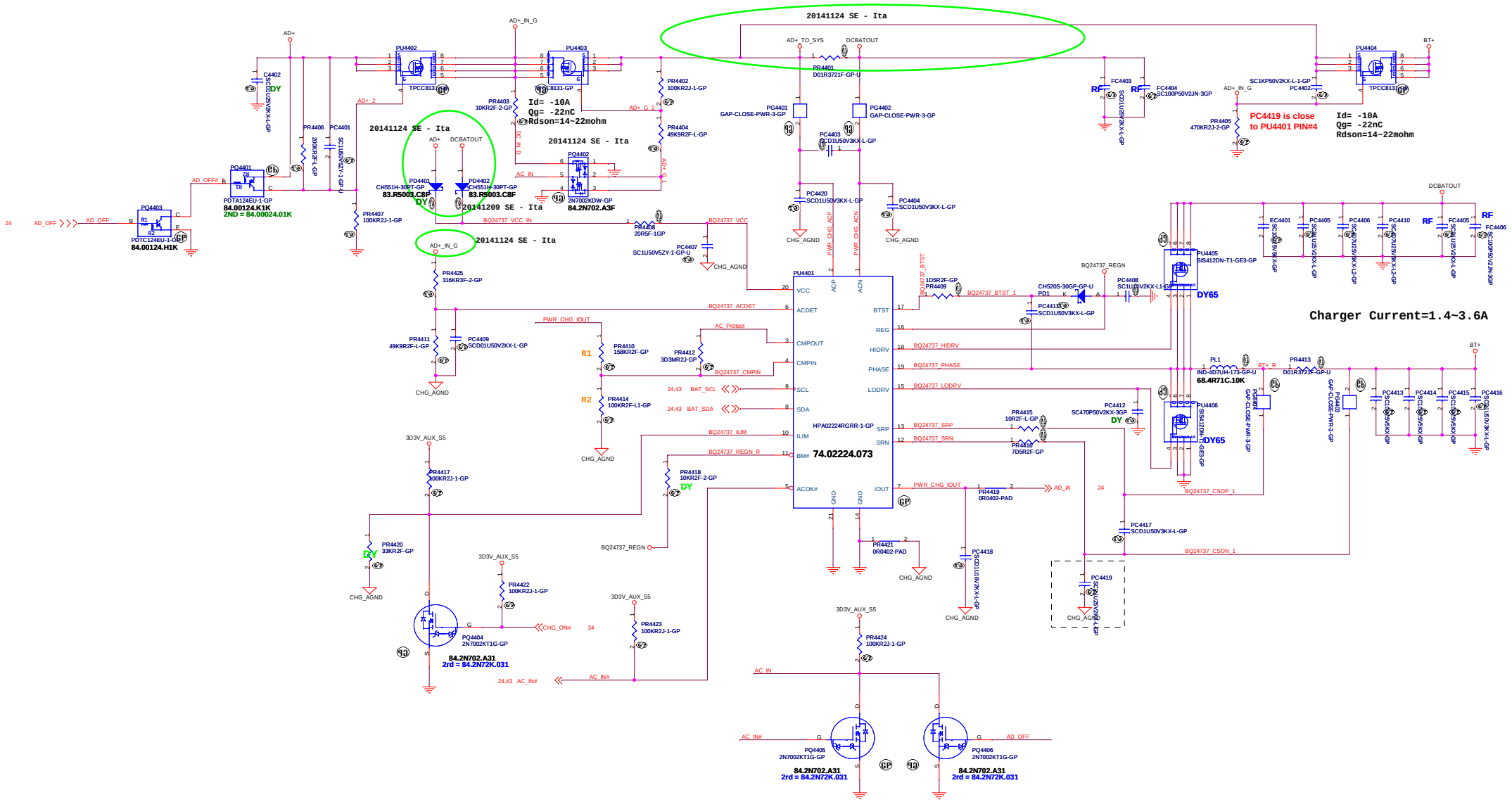
SSID = Charger



20140812 Change Charge solution follow Reacher.

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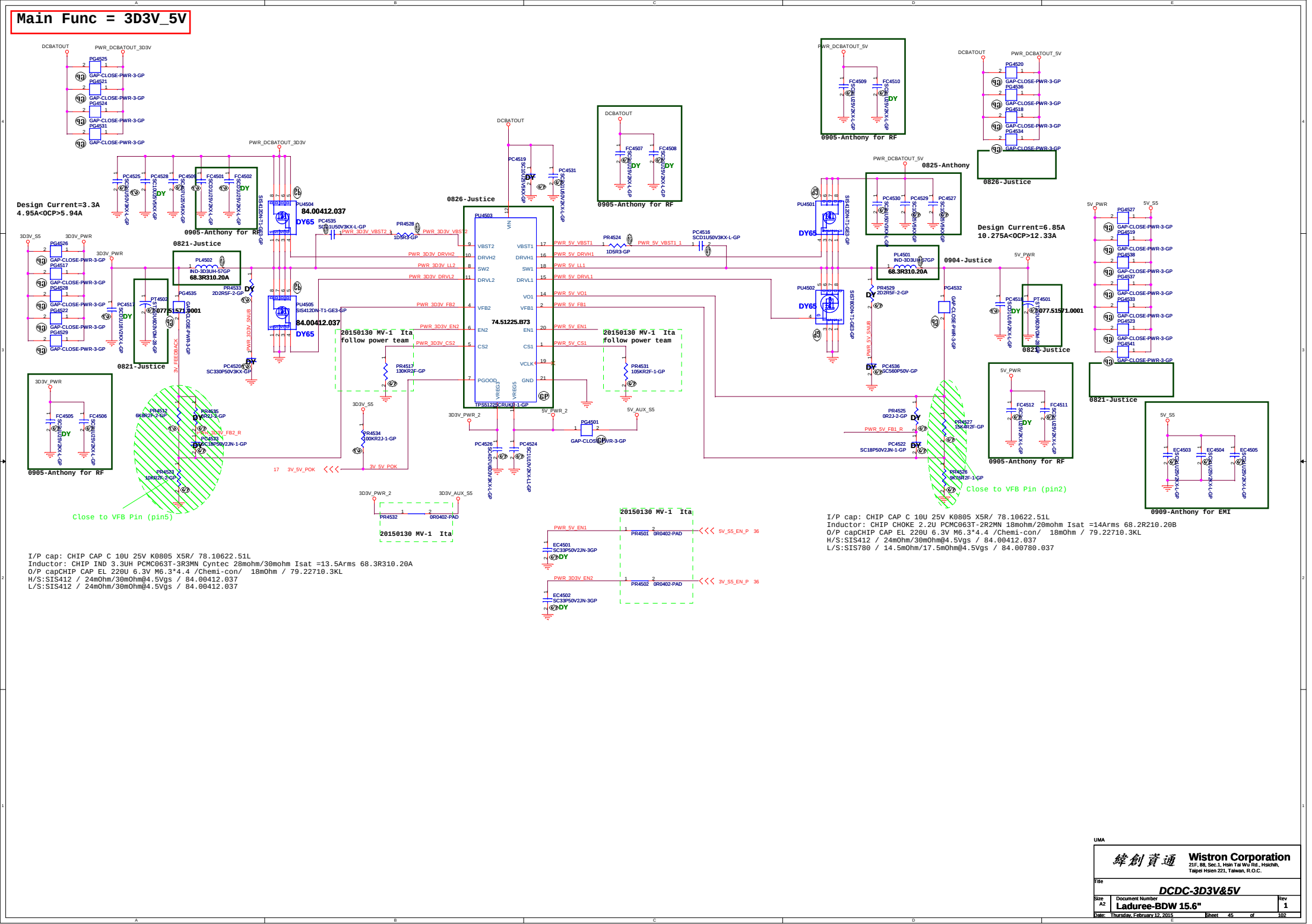
Title: HPA02224RGRR

Size	Document Number	Rev
A2	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 44 of 102

Main Func = 3D3V_5V



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Title: DCDC-3D3V&5V

Size	Document Number	Rev
A2	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 45 of 102

SSID = CPU.Regulator

PR4602 NTC-100K-10-GP-U 69.60037.031 2nd = 69.60028.011

PR4606 9K09R2F-GP

PC4603 SC1KP50V2KX-L-1-GP

PC4602 SC4700P50V2KX-1GP

330KR2F-L-GP PR4607

39KR2F-GP PR4608

PR4612 DY 75R2F-2-GP

PR4613 39KR2F-GP

PR4615 10KR3F-L-GP

PWR_VCC_VREF

PR4603 75R2F-2-GP DY

PR4604 680KR2F-GP

PR4605 56KR2F-GP

PR4609 150KR2F-L-GP

PR4610 100KR2F-L1-GP

PR4611 30KR2F-GP

PWR_VCC_B-RAMP

PWR_VCC_F-Imax

PWR_VCC_O-USR

PWR_VCC_SLEWA

PWR_VCC_VBAT

DCBATOUT

PWR_VCC_THERM

PWR_VCC_IMON

PWR_VCC_OCP-1

1D05V_VCCST

IMVP_PWRGD

PR4614 DY 2KR2F-L1-GP

PU4601 TPS51624RSMR-GP-U1

74.51624.073

20150204 MV-1 Ita

PR4617 0R0402-PAD

IMVP_VRON

H_VR_EN 7

3D3V_S0

PR4616 1KR2J-1-GP

PR4601 change to 1k ohm when D4610 mount

20150210 MV-1 Ita

PR4601 0R0402-PAD

IMVP_PWRGD 7,36

D4610 DY BAT54C-11-GP

C4610 SCD1U16V2KX-L-GP DY

47 PWR_VCC_CSP1

47 PWR_VCC_CSN1

3D3V_S5

PR4618 PWR_VCC_CSP2 0R0402-PAD

PR4619 PWR_VCC_PU3 0R0402-PAD

9 VSS_SENSE

PR4620 PWR_VCC_GFB 0R0402-PAD

7 VCC_SENSE

PR4621 PWR_VCC_VFB 0R0402-PAD

20150204 MV-1 Ita

CSP1 CSN1 CSN2 CSP2 NC#21 NC#22 GFB VFB

VBAT SLEWA THERM IMON OCP-I BOOT F-IMAX O-USR

VR_ON SKIP# PWM1 PWM2 MODE PGOOD VDD VDIO

DROOP COMP VREF VSA GND VR_HOT# VCLK ALERT# GND

IMVP_VRON

PWR_VCC_SKIP# 47

PWR_VCC_PWM1 47

PR4627 DY 100KR2F-L-GP

IMVP_PWRGD_R

PWR_VCC_VDD

PR4221 = 1R

2012.0529 . wayler

PR4622 1R2F-GP

3D3V_S5

PC4604 SCD1U10V2KX-L1-GP

75.00054.T7D

2nd = 75.00054.A7D

3rd = 75.00054.F7D

PWR_VCC_DROOP

SC100P50V2JN-3GP PC4606 DY

PWR_VCC_COMP

PR4624 10KR2F-2-GP

PWR_VCC_VREF

PR4625 4K75R2F-1-GP

PC4607 SCD33U6D3V2KX-1-GP

PWR_VCC_COMP_R

PC4608 SC1500P50V2KX-2GP

PR4628 4K75R2F-1-GP

PWR_VCC_VSA

H_CPU_SVIDDAT 7

VR_SVID_ALERT# 7

H_CPU_SVIDCLK 7

H_PROCHOT# 4,24

5V_S5

PR4629 10R2F-L-GP

PC4601 SC1U10V2KX-L1-GP

1D05V_VCCST

PC4605 SCD1U16V2KX-L-GP

PR4623 110R2F-GP

H_CPU_SVIDDAT

PR4626 54D9R2F-L1-GP

H_CPU_SVIDCLK

PC4620 SC8P50V2DN-1GP

Close to PU4601

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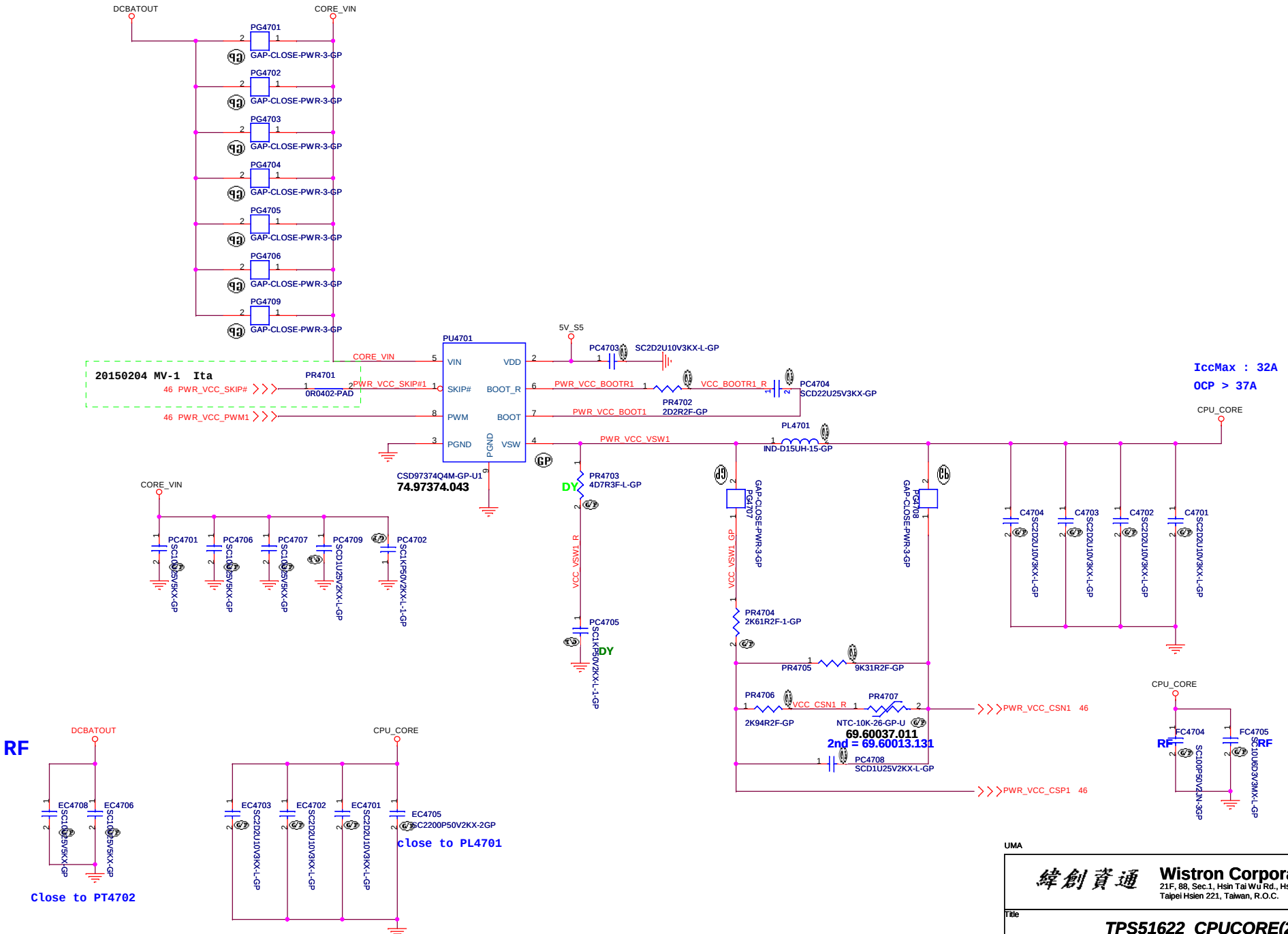
Title: TPS51622_CPUCORE(1/2)

Size: A3 | Document Number: Laduree-BDW 15.6" | Rev: 1

Date: Thursday, February 12, 2015 | Sheet 46 of 102



UMA

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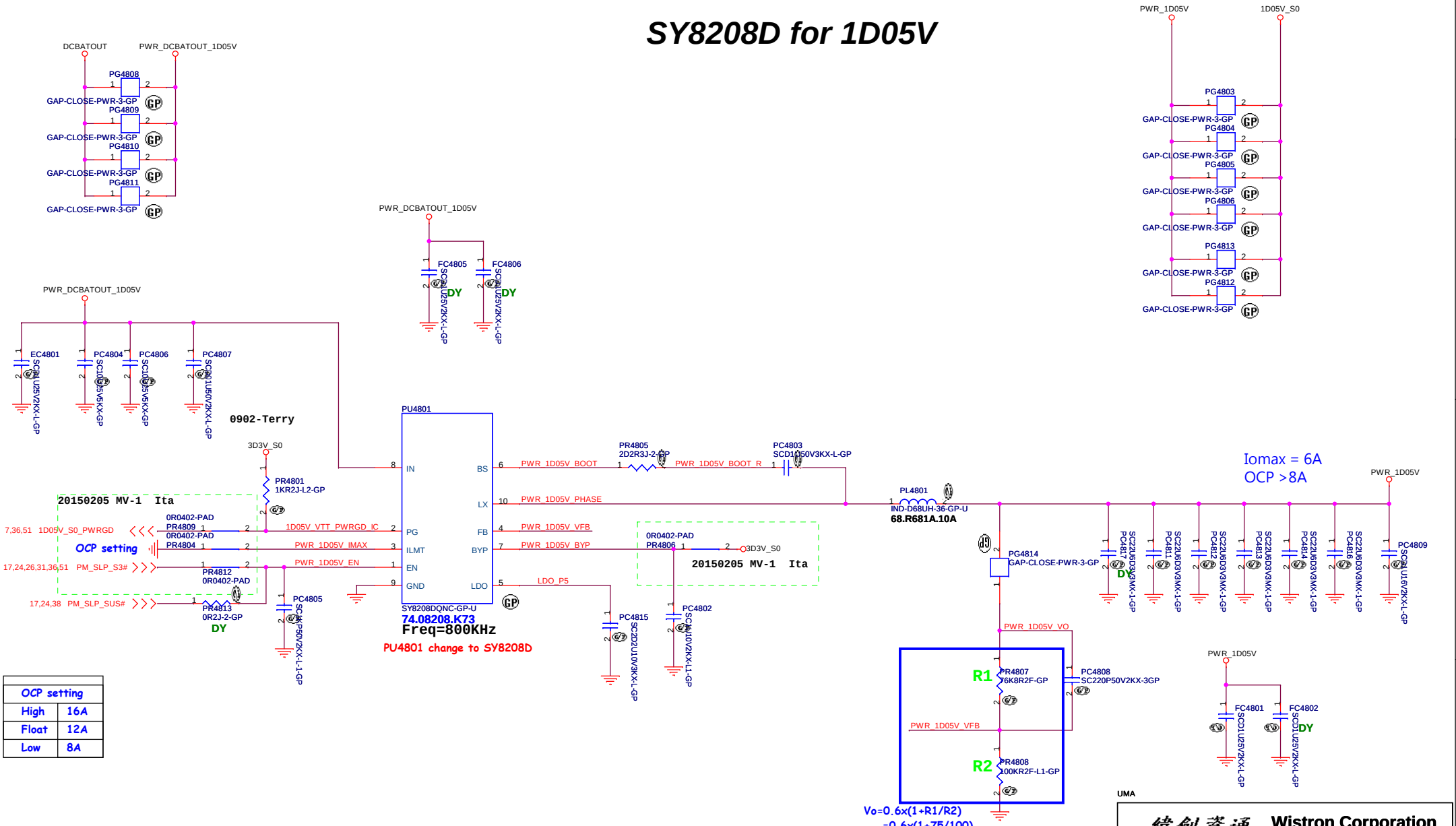
Title	TPS51622_CPUCORE(2/2)	
Size A3	Document Number Laduree-BDW 15.6"	Rev 1
Date: Thursday, February 12, 2015	Sheet 47 of 102	

SSID = PWR.Plane.Regulator_1p05v

SY8208D for 1D05V



OCP setting	
High	16A
Float	12A
Low	8A

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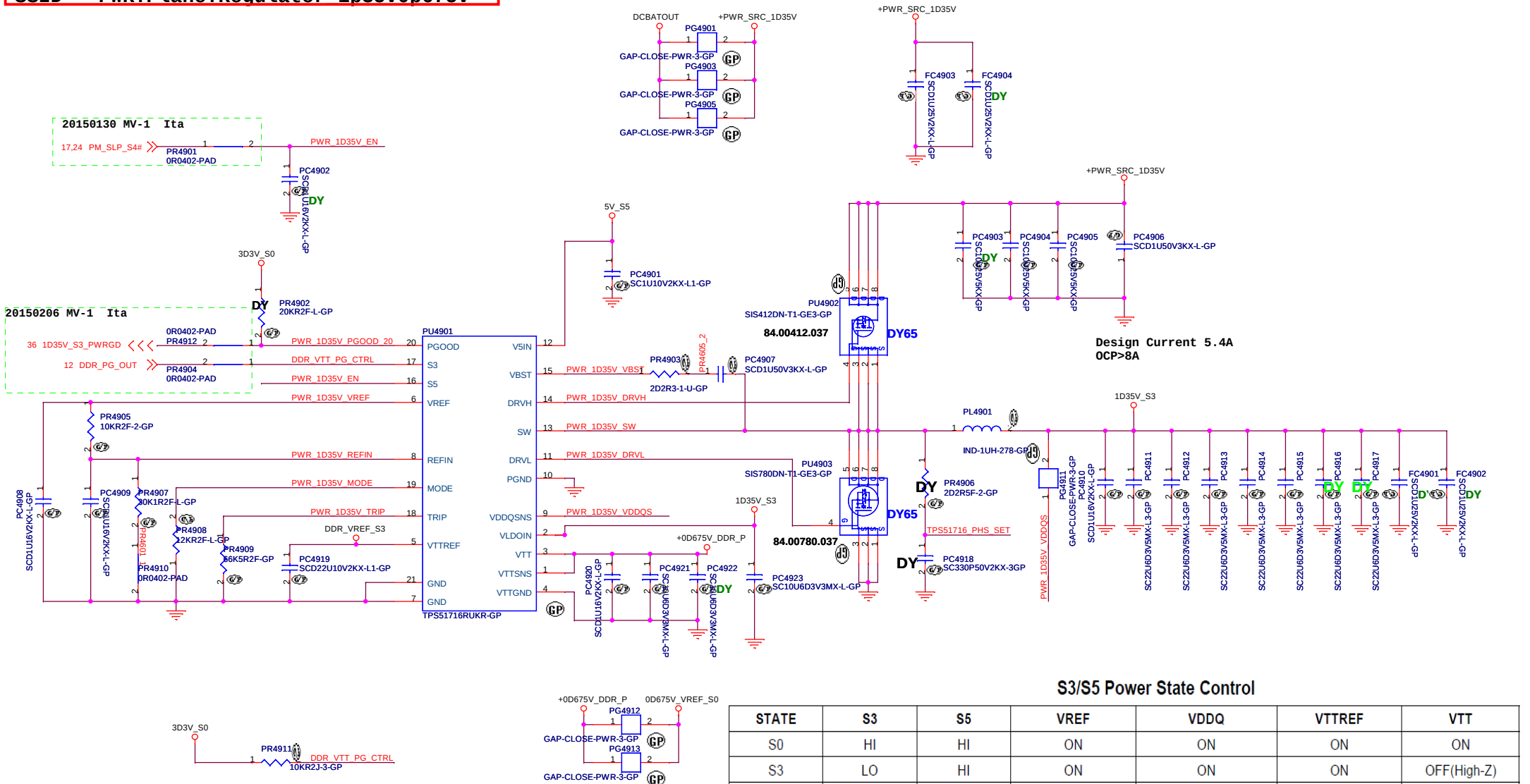
Title: *SY8208D for 1D05V*

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 48 of 102

SSID = PWR.Plane.Regulator_1p35v0p675v



S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	CONTROL MODE	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	33	D-CAP2	500	Non-Tracking
2	22		670	
1	12		670	Tracking
0	1		500	

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Title: ***TPS51716(VDDQ_VTT)***

Size: A3 | Document Number: **Laduree-BDW 15.6"** | Rev: 1

Date: Thursday, February 12, 2015 | Sheet 49 of 102

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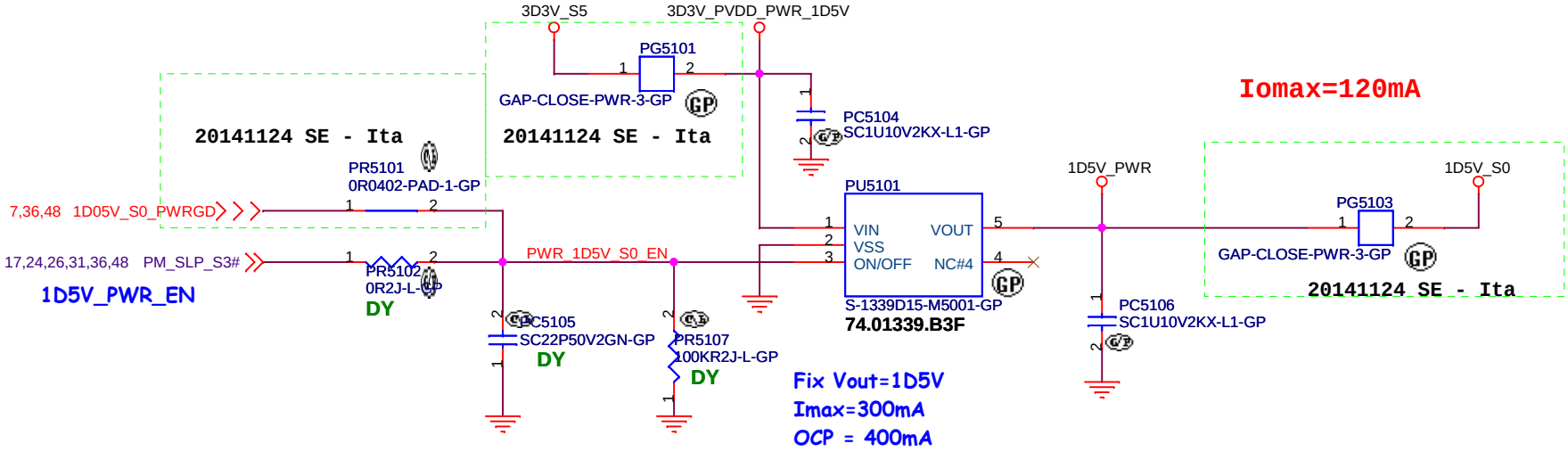
Title

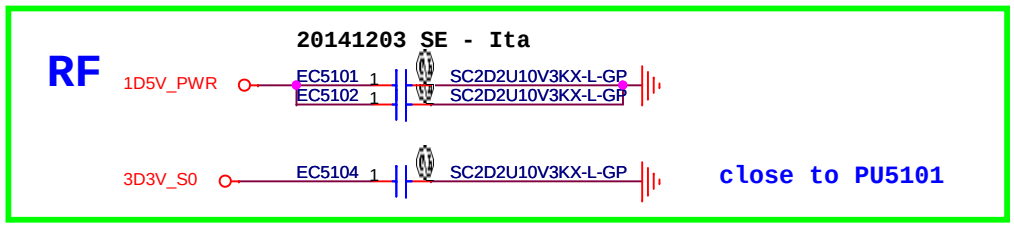
(Reserved)1D8V_S0

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Friday, January 30, 2015 Sheet 50 of 102

SSID = 1D5V_S0





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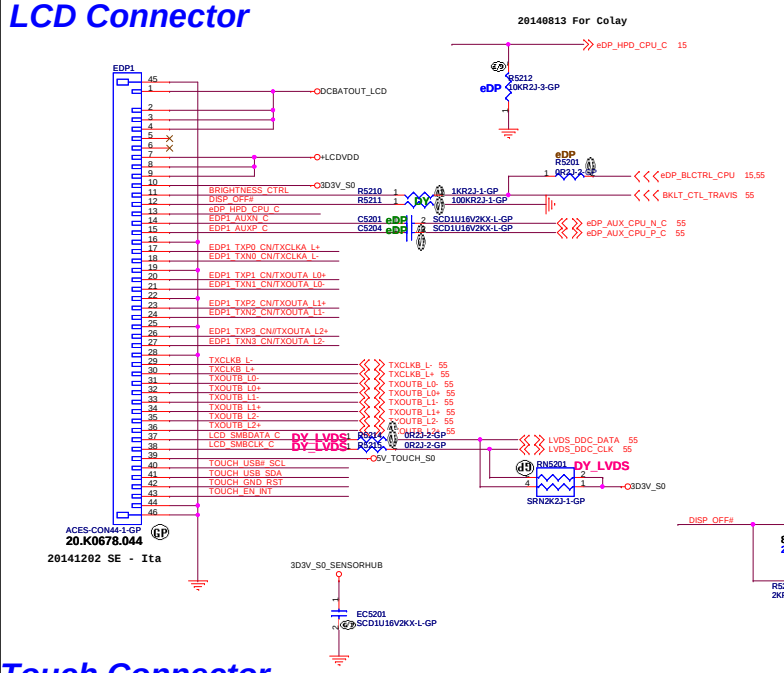
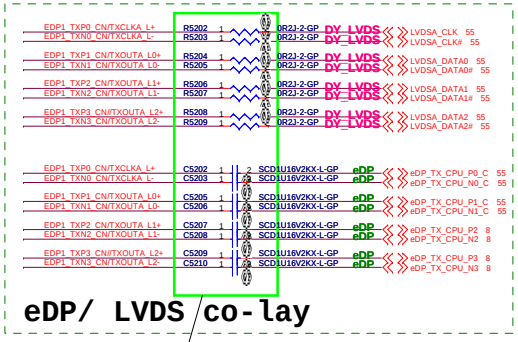
Title	*1D5V_S0*	
Size A4	Document Number **Laduree-BDW 15.6"**	Rev 1
Date: Thursday, February 12, 2015	Sheet 51 of 102	

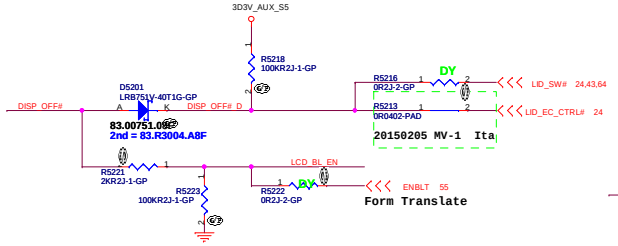
LCD Connector



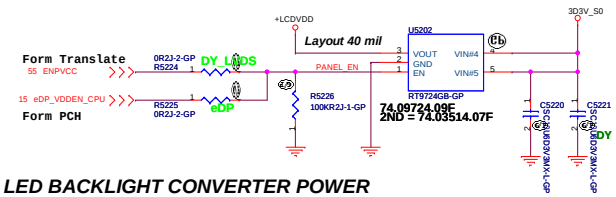


eDP/ LVDS co-lay

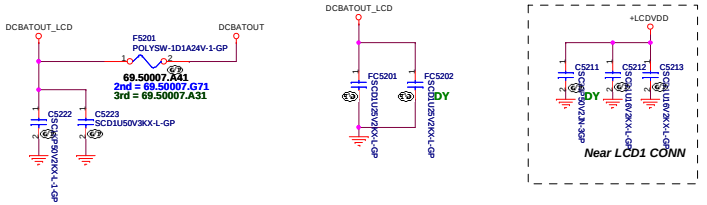
Close to LCD Connector



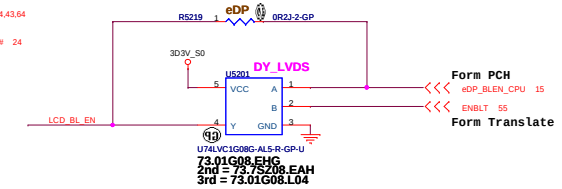
LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER



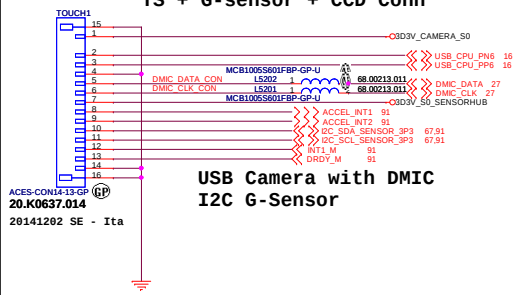
0905-Anthony for RF



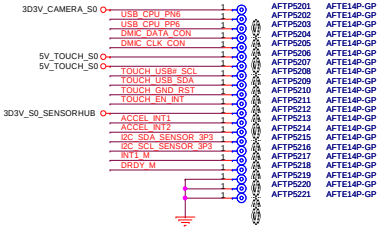
Touch Connector

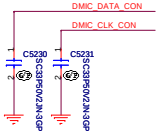
20141017 SC - Ita

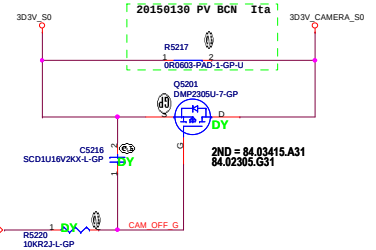
TS + G-sensor + CCD Conn

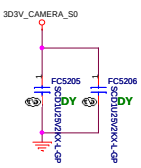


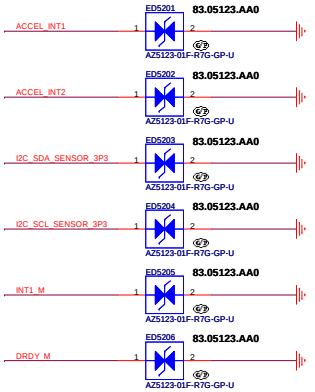
USB Camera with DMIC
I2C G-Sensor

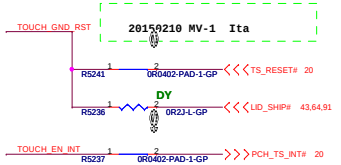


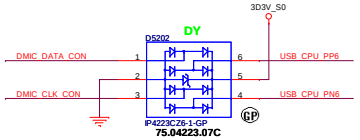


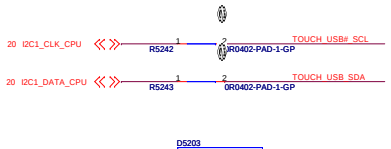


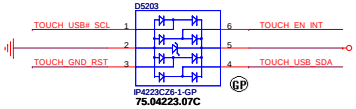


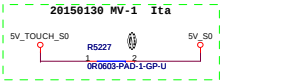




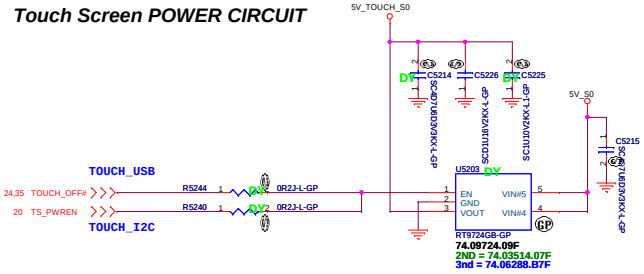


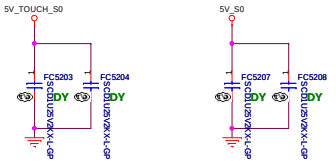






Touch Screen POWER CIRCUIT





UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: EDP Connector		
Size: A2	Document Number: Laduree-BDW 15.6"	Rev: 1
Date: Thursday, February 12, 2015	Sheet 52 of 102	

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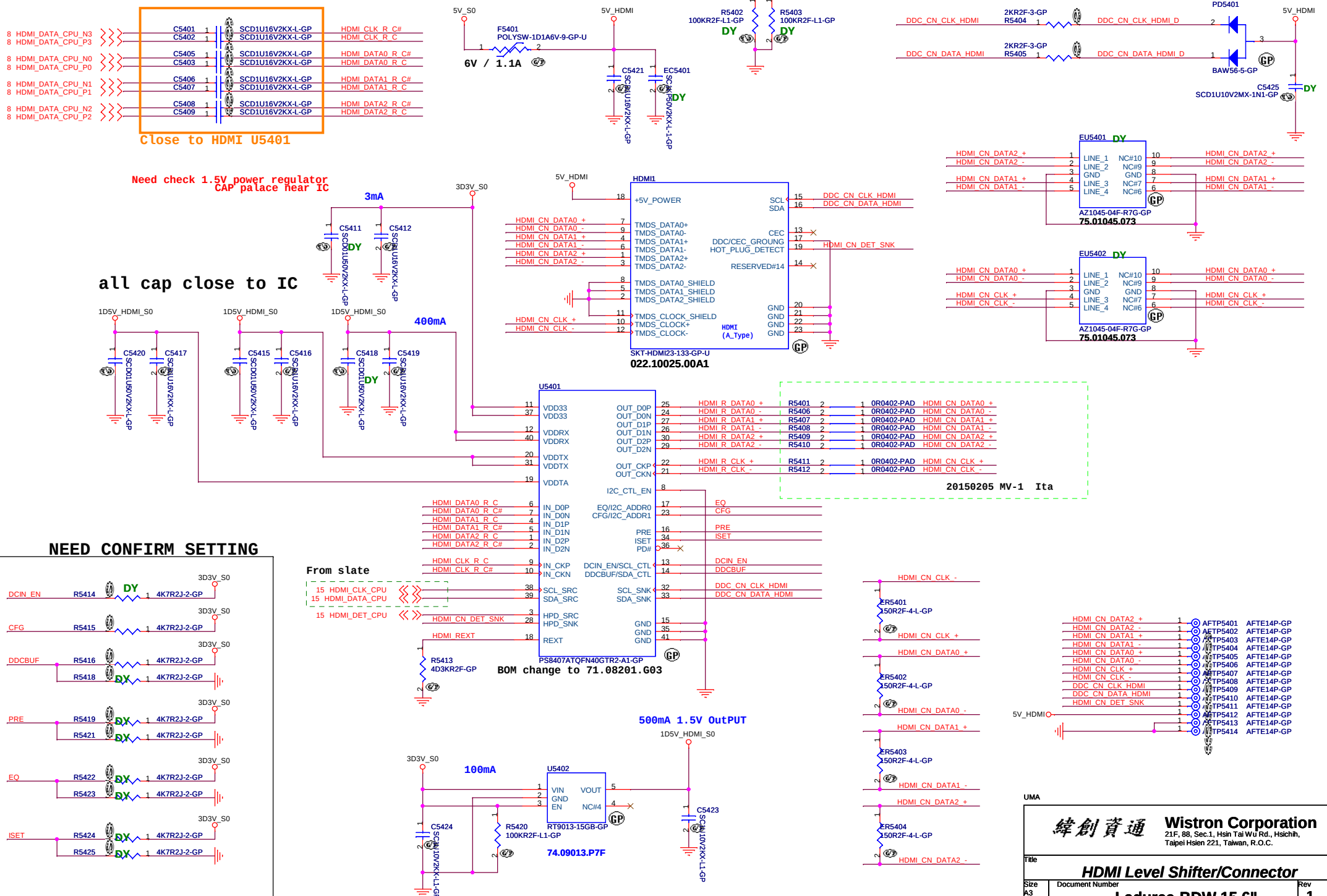
Title

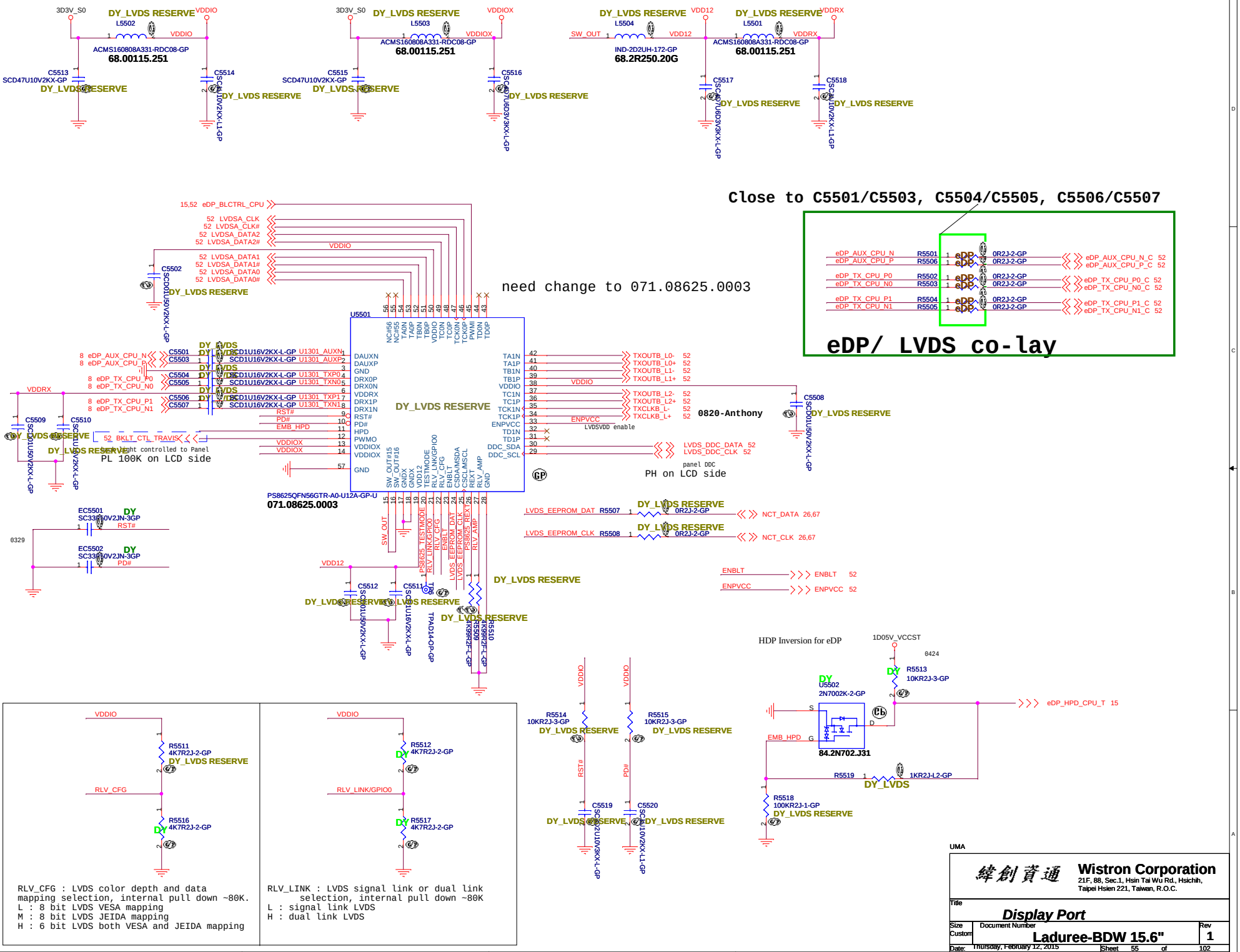
CRT Board Connector

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Friday, January 30, 2015 Sheet 53 of 102

HDMI Connector




Close to C5501/C5503, C5504/C5505, C5506/C5507
eDP/ LVDS co-lay
need change to 071.08625.0003
PS8625QFN56GTR-A0-U12A-GP-U
071.08625.0003
PL 100K on LCD side
PH on LCD side
0820-Anthony
HDP Inversion for eDP
RLV_CFG : LVDS color depth and data mapping selection, internal pull down ~80K.
L : 8 bit LVDS VESA mapping
M : 8 bit LVDS JEIDA mapping
H : 6 bit LVDS both VESA and JEIDA mapping
RLV_LINK : LVDS signal link or dual link selection, internal pull down ~80K
L : signal link LVDS
H : dual link LVDS
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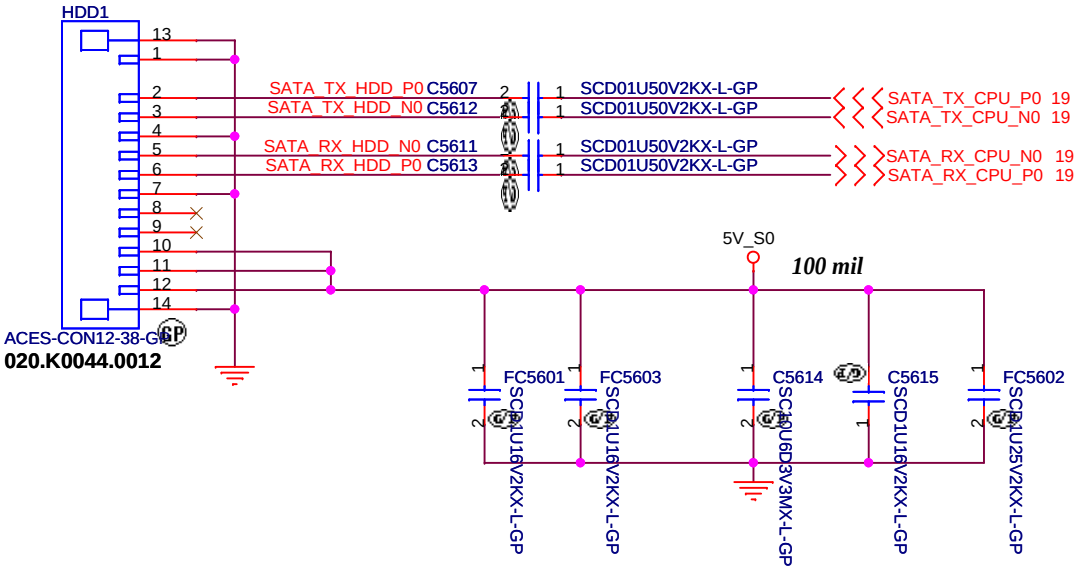
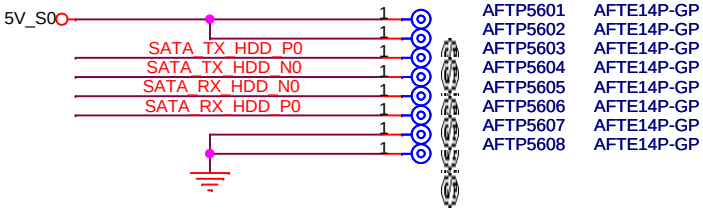
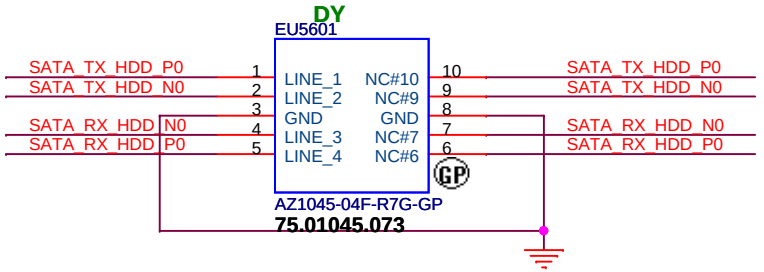
Display Port
Laduree-BDW 15.6"
Thursday, February 12, 2015

SSID = SATA

SATA HDD Connector







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Title: ***HDD / ODD / NGFF_SSD***

Size	Document Number	Rev
A4	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 56 of 102

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Title

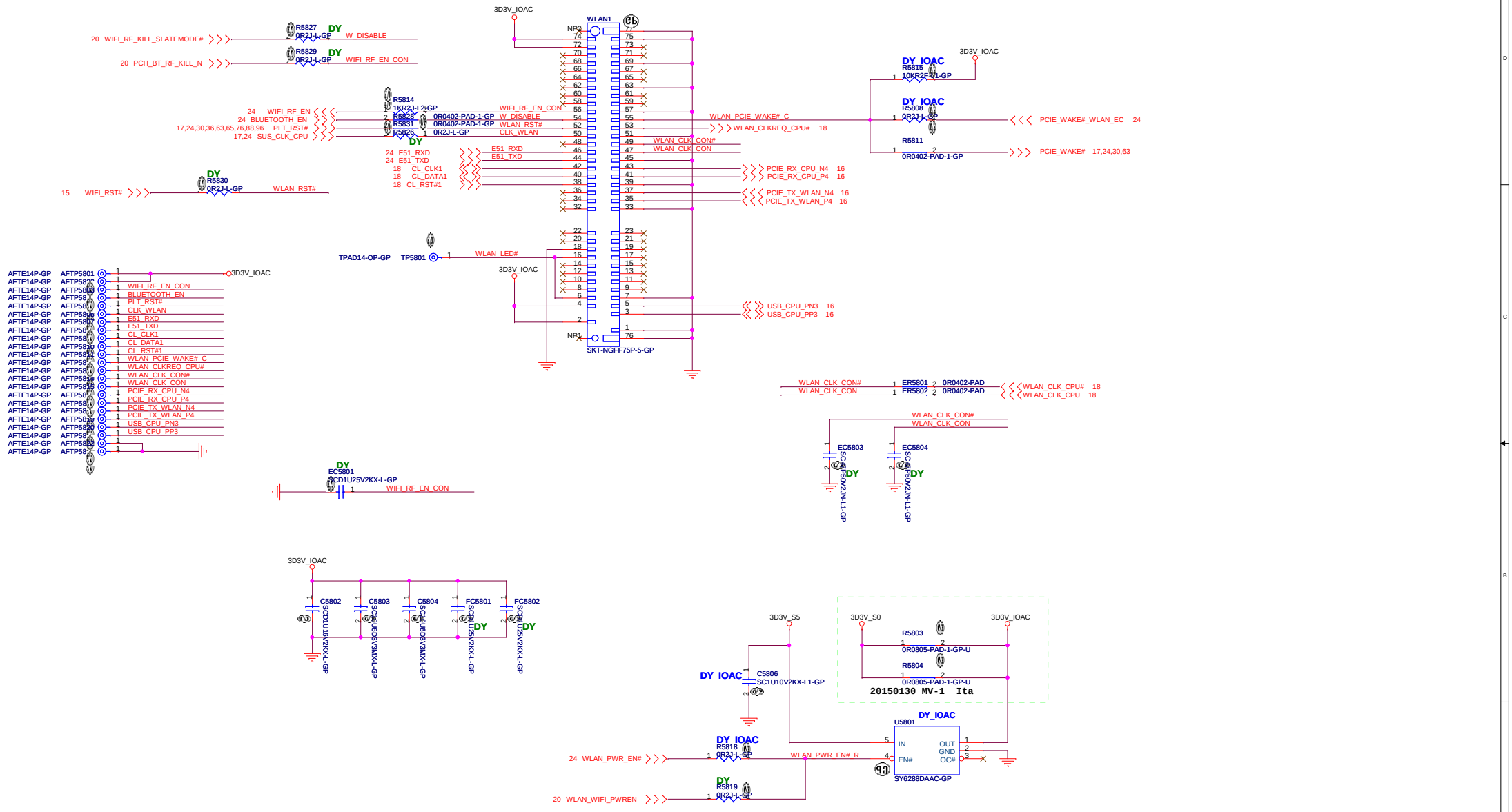
E-SATA

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

Date: Friday, January 30, 2015 Sheet 57 of 102

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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Title: MINICARD(WLAN)

Size: Custom | Document Number: Laduree-BDW 15.6" | Rev: 1

Date: Thursday, February 12, 2015 | Sheet 58 of 102

UMA

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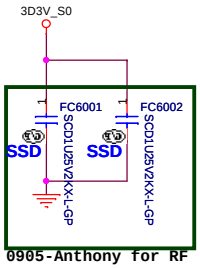
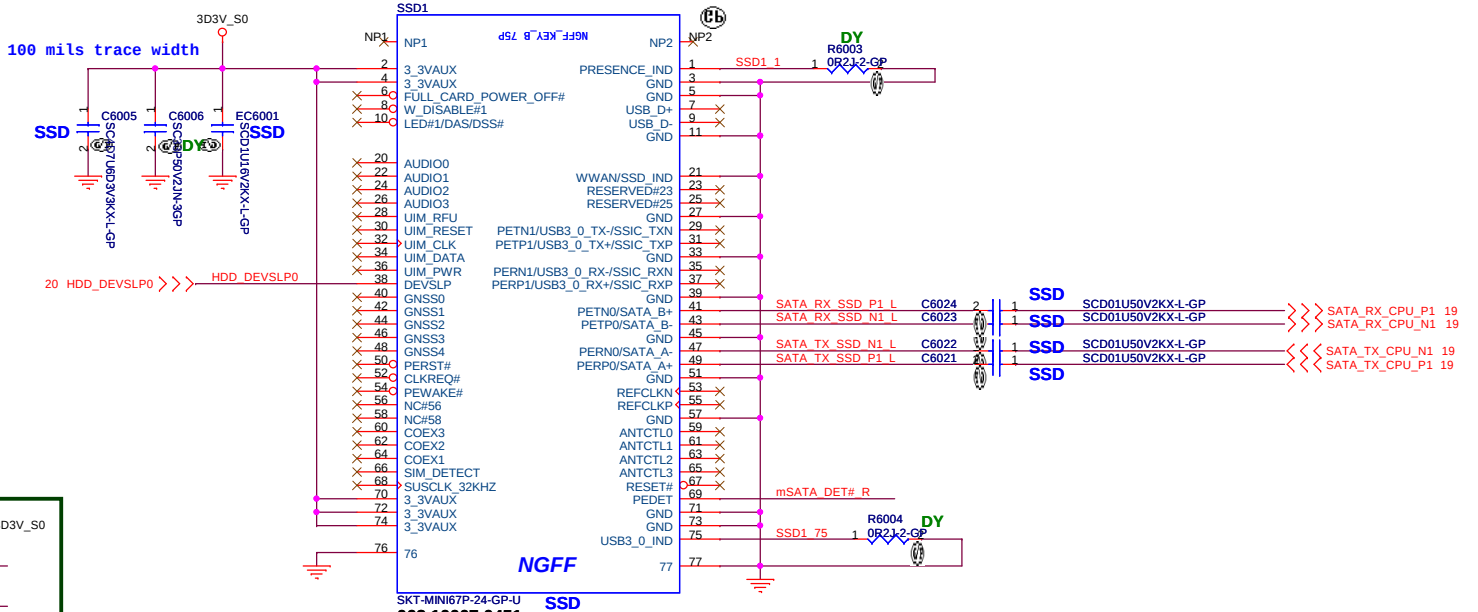
Title: ***WWAN CONN(Reserver)***

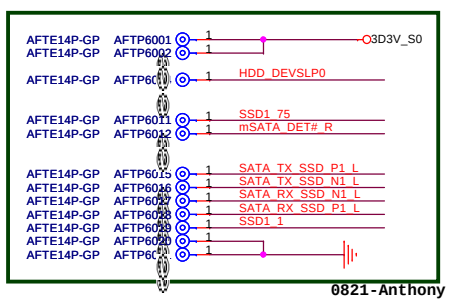
Size	Document Number	Rev
A3	**Laduree-BDW 15.6"**	1

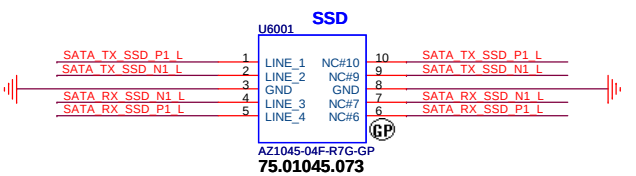
Date: Friday, January 30, 2015 Sheet 59 of 102

SSID = SATA SSD

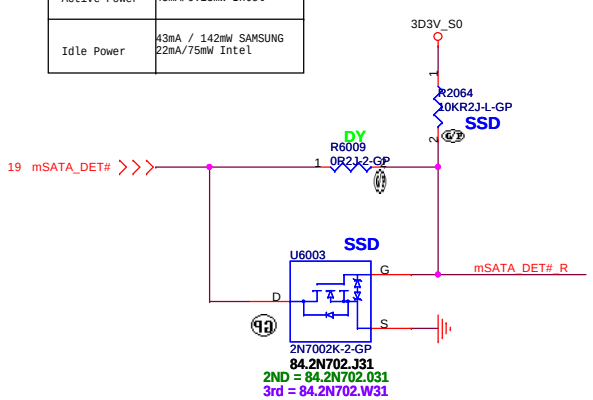








power supply	3.3V
Active Power	50mA / 0.165W SAMSUNG 45mA/0.15mW Intel
Idle Power	43mA / 142mW SAMSUNG 22mA/75mW Intel



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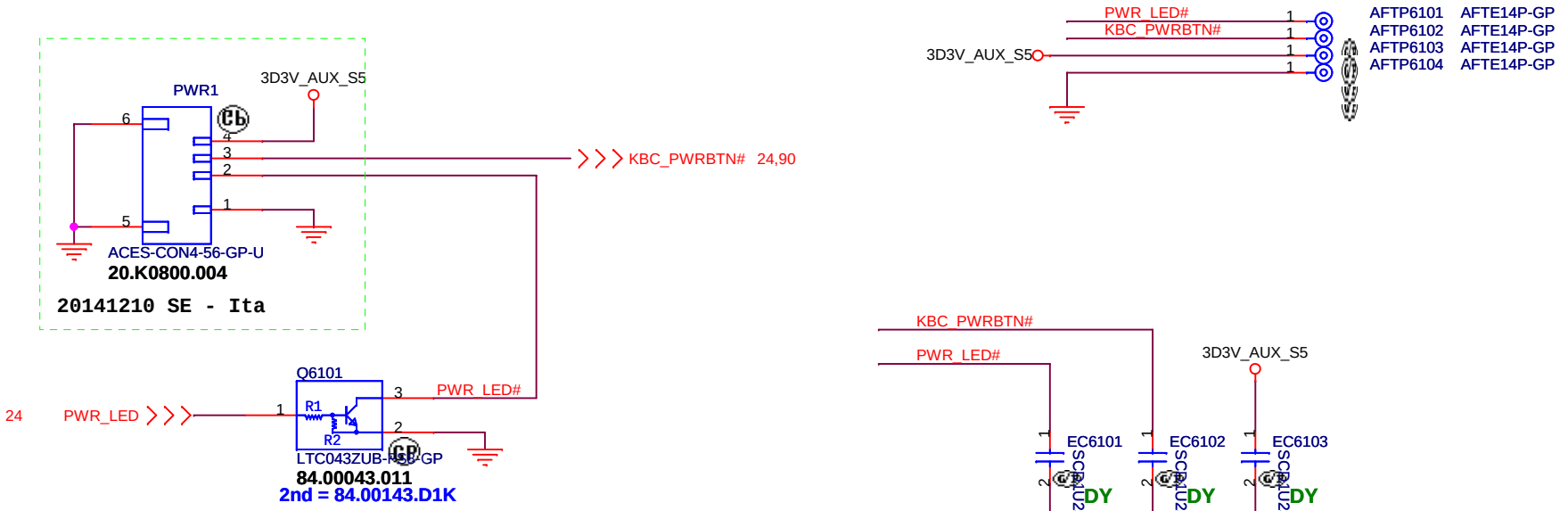
Title: ***mSATA Connector***

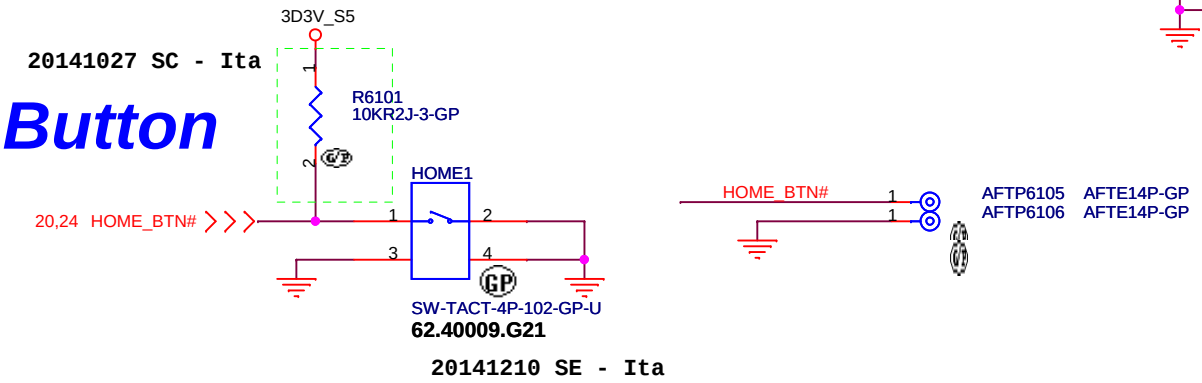
Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

Date: Thursday, February 12, 2015 Sheet 60 of 102

Power Button



Home Button



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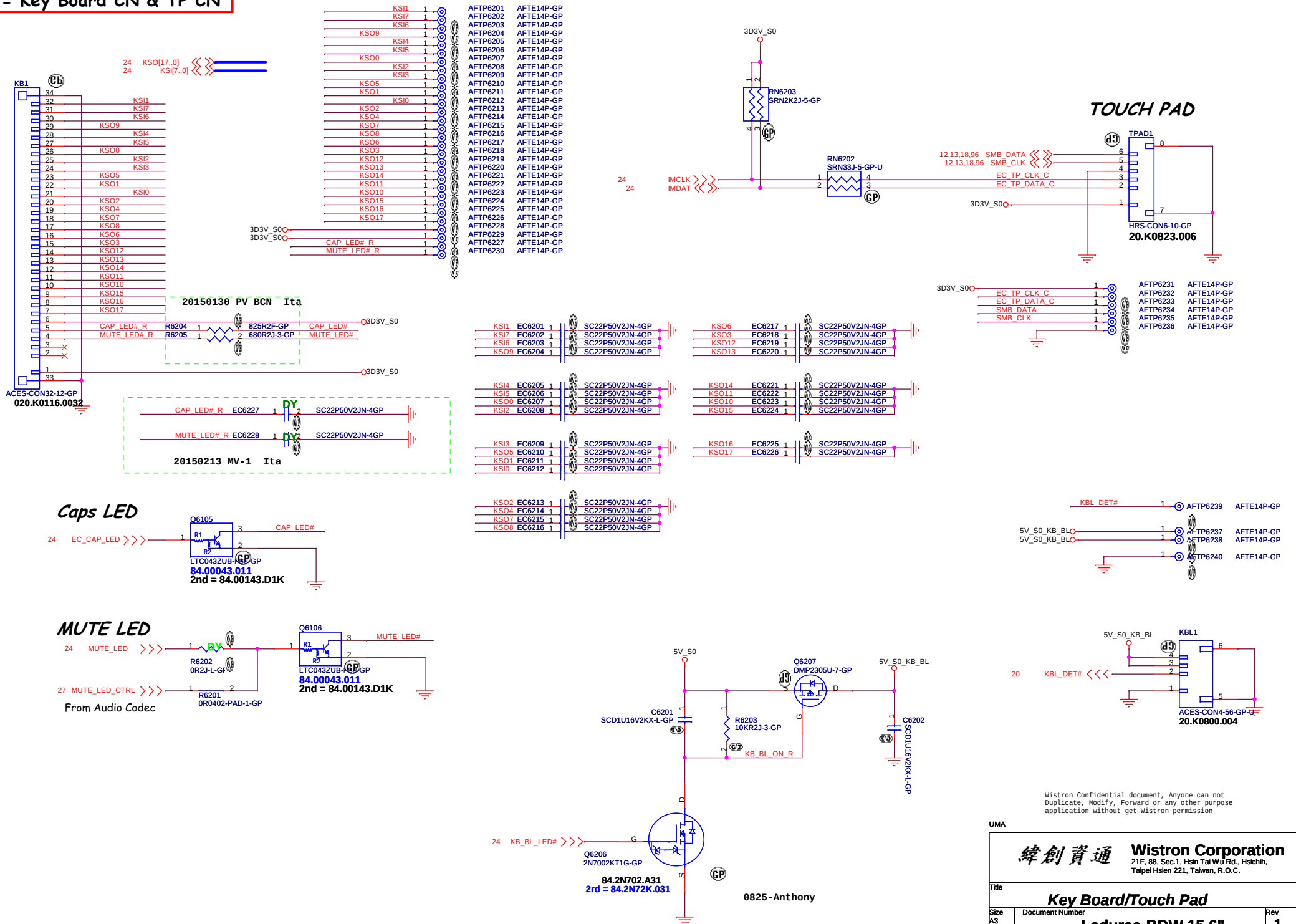
Title: ***LED Bard/Power Button***

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

Date: Thursday, February 12, 2015 Sheet 61 of 102

SSID = Key Board CN & TP CN



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緯創資通 **Wistron Corporation**
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Title: **Key Board/Touch Pad**

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

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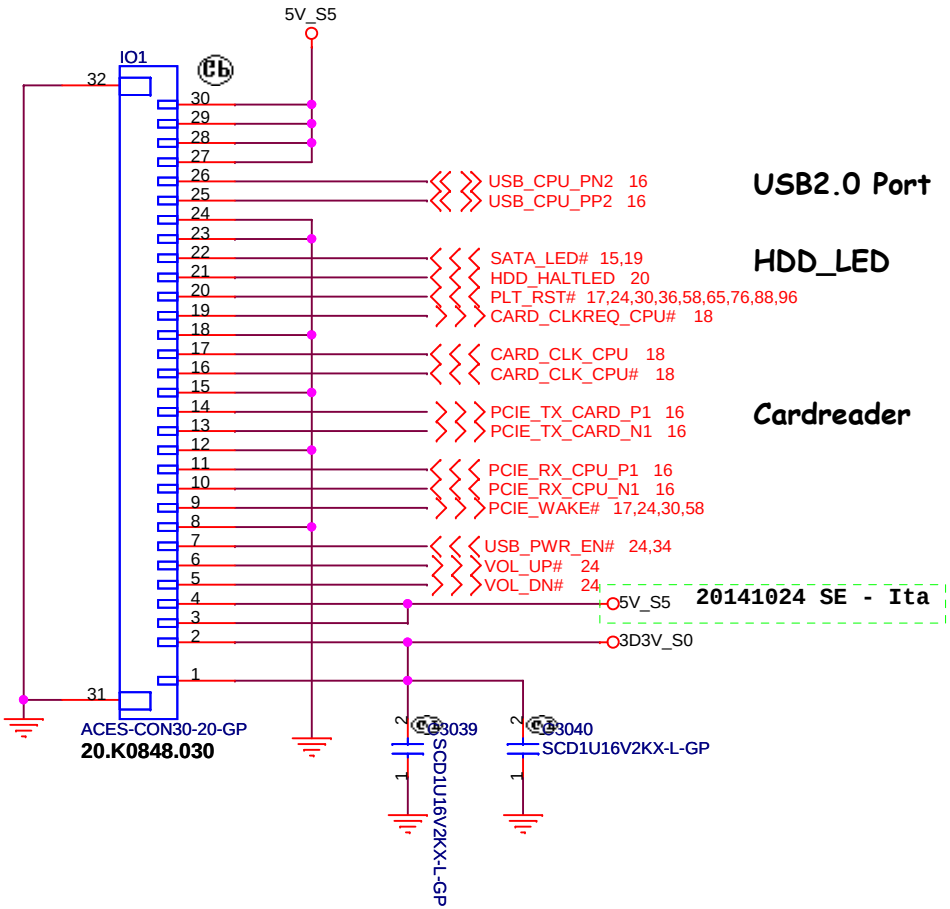

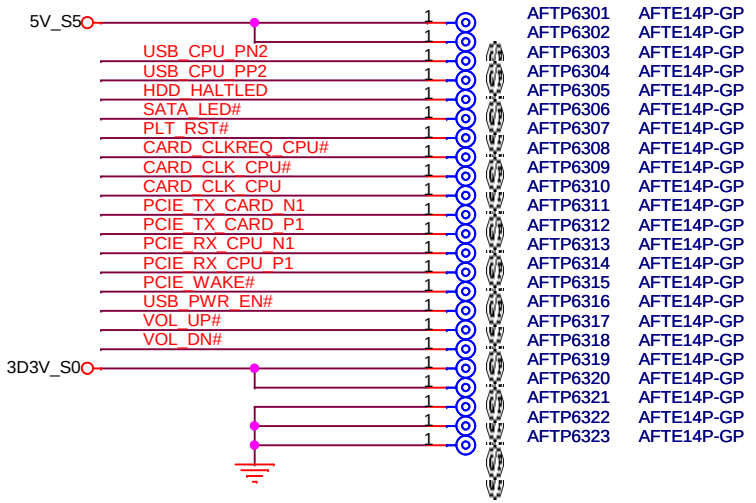

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Title: ***IO Board Connector***

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

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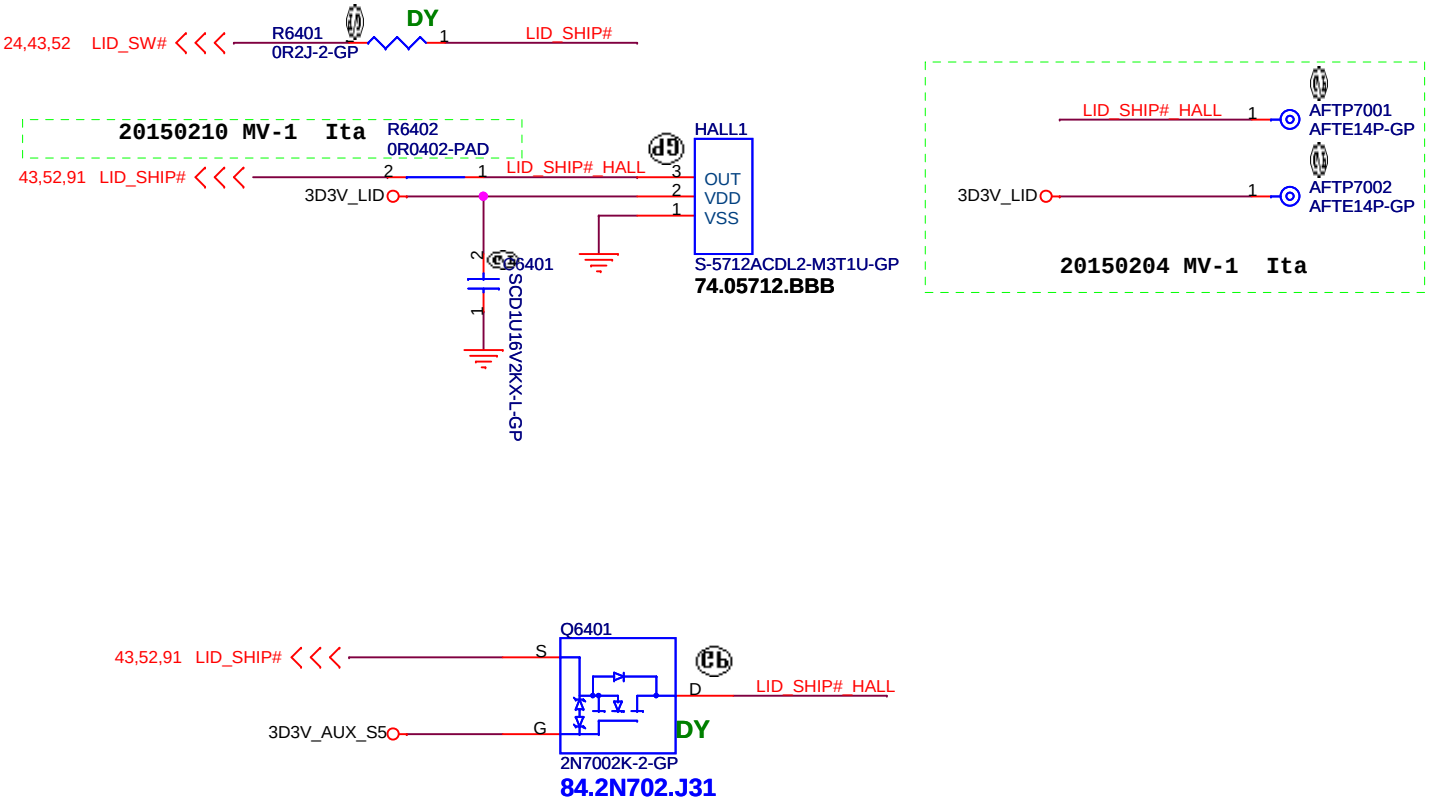

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緯創資通 **Wistron Corporation**
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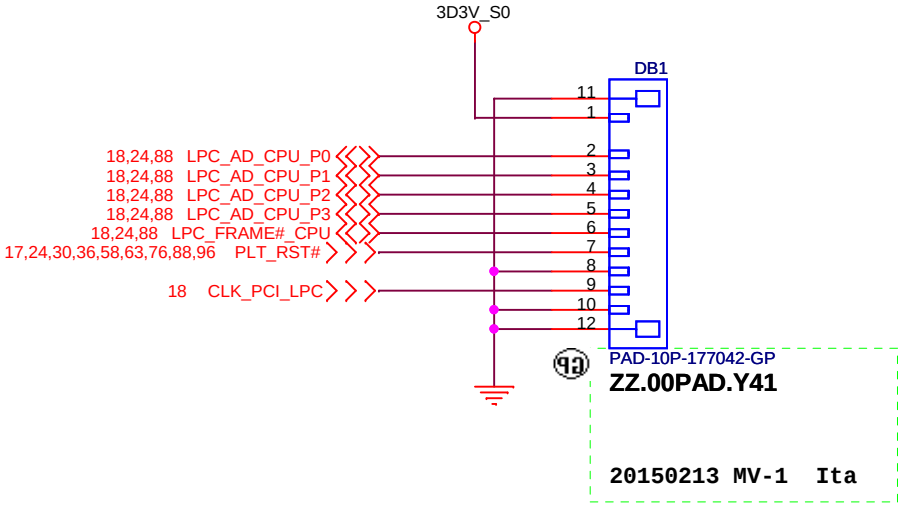
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

Date: Thursday, February 12, 2015 Sheet 64 of 102



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Title: ***Dubug connector***

Size	Document Number	Rev
A4	**Laduree-BDW 15.6"**	1

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緯創資通 **Wistron Corporation**

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Title

Reserve

Size	Document Number	Rev
A3	**Laduree-BDW 15.6"**	1

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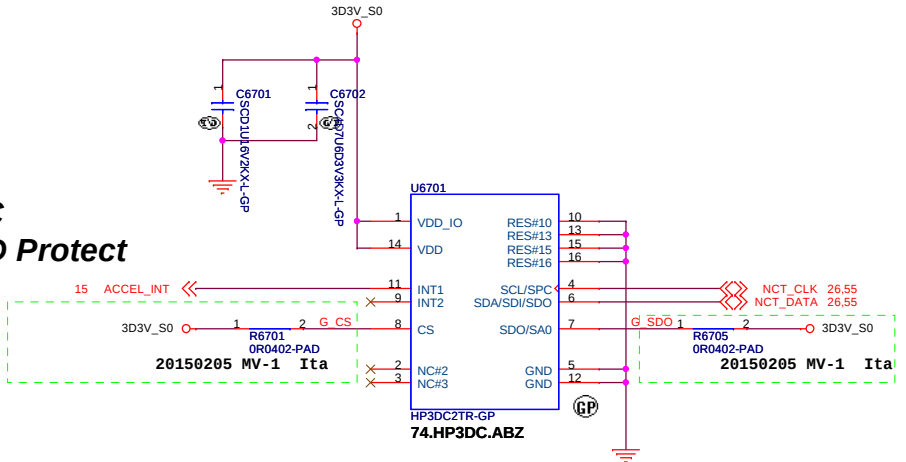
ACCELEROMETER

To KBC for HDD Protect

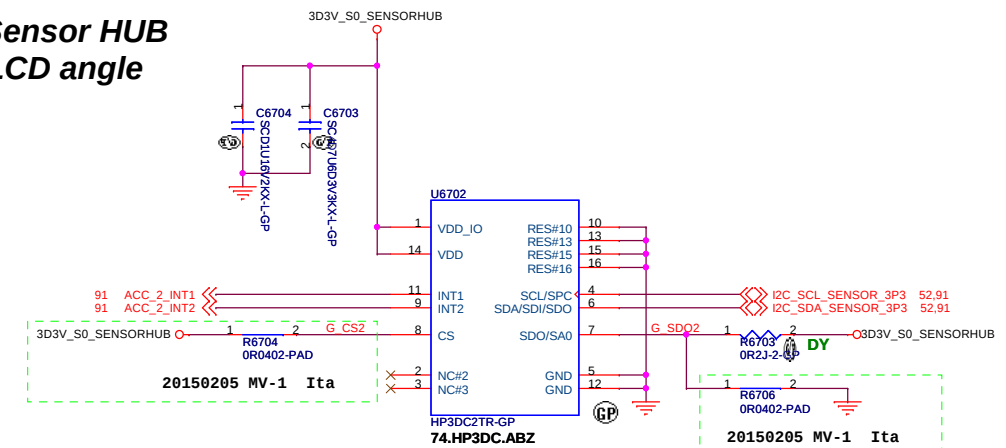


Must be placed in the center of the system

Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

To Sensor HUB for LCD angle



Must be placed in the center of the system

Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

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Title: **G Sensor**

Size	Document Number	Rev
A3	Laduree-BDW 15.6"	1

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UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Thunderbolt (1/5)***

Size	Document Number	Rev
Custom	Laduree-BDW 15.6"	1

Date: Friday, January 30, 2015 Sheet 68 of 102

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Thunderbolt (2/5)***

Size	Document Number	Rev
Custom	Laduree-BDW 15.6"	1

Date: Friday, January 30, 2015 Sheet 69 of 102

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緯創資通

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Title: ***Thunderbolt (3/5)***

Size	Document Number	Rev
Custom	Laduree-BDW 15.6"	1
Date: Friday, January 30, 2015	Sheet 70 of 102	

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Thunderbolt (4/5)***

Size	Document Number	Rev
Custom	**Laduree-BDW 15.6"**	1

Date: Friday, January 30, 2015 Sheet 71 of 102

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緯創資通

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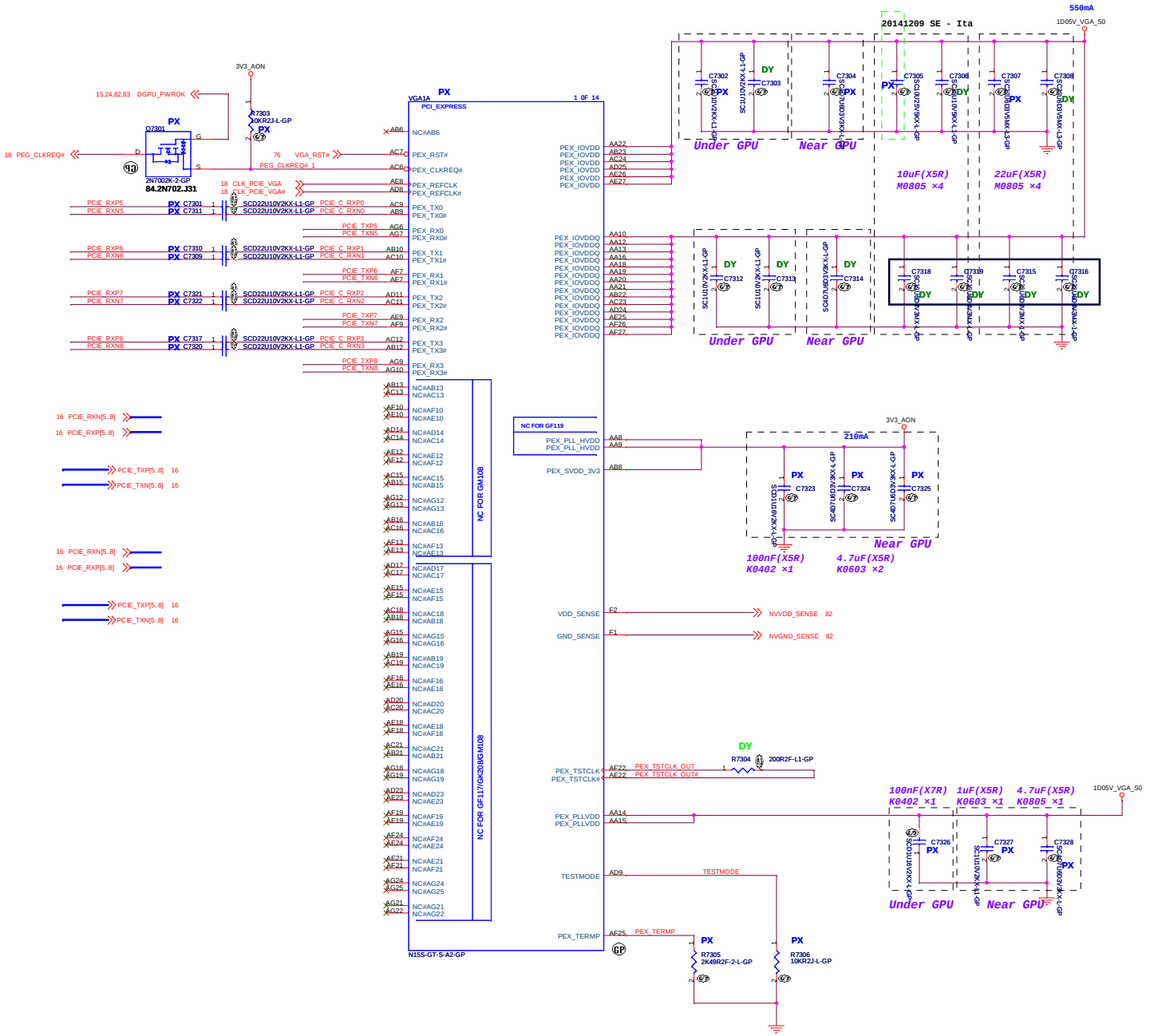
Title

Thunderbolt (5/5)

Size	Document Number	Rev
A4	Laduree-BDW 15.6"	1

Date: Friday, January 30, 2015 Sheet 72 of 102



3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128	1.0 µF	X6S	0402	4	Under GPU
GB3B-256	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

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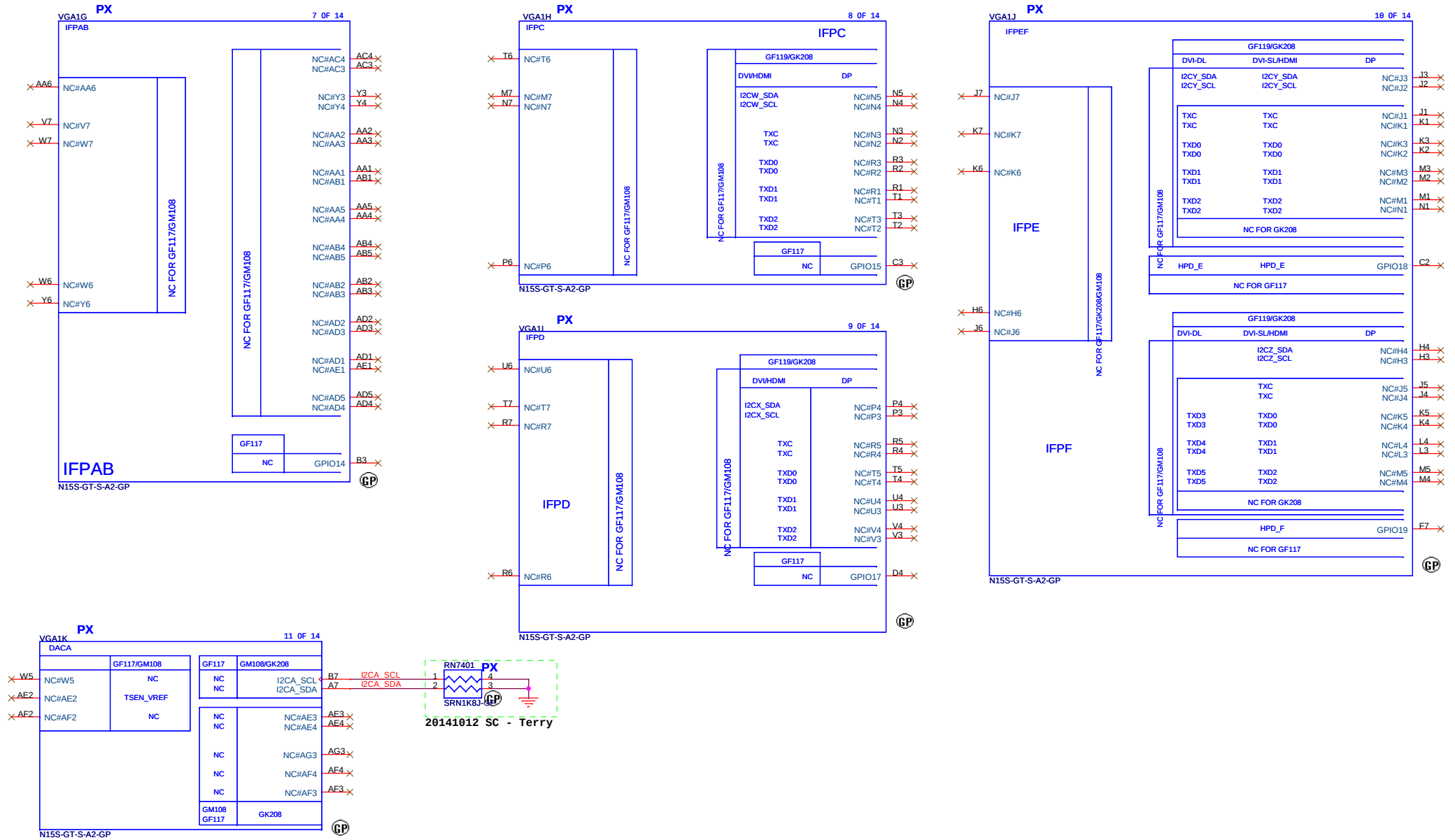
Title: GPU_PEG (1/5)

Size: A2 | Document Number: Laduree-BDW 15.6" | Rev: 1

Date: Thursday, February 12, 2015 | Sheet 73 of 102


PX
VGA1G
7 OF 14
IFPAB
NC#AA6
NC#V7
NC#W7
NC#W6
NC#Y6
NC FOR GF117/GM108
NC#AC4
NC#AC3
NC#Y3
NC#Y4
NC#AA2
NC#AA3
NC#AA1
NC#AB1
NC#AA5
NC#AA4
NC#AB4
NC#AB5
NC#AB2
NC#AB3
NC#AD2
NC#AD3
NC#AD1
NC#AE1
NC#AD5
NC#AD4
GF117
NC
GPIO14
IFPAB
N15S-GT-S-A2-GP
VGA1H
8 OF 14
IFPC
NC#T6
NC#M7
NC#N7
NC#P6
GF119/GK208
DVI/HDMI
DP
I2CW_SDA
I2CW_SCL
TXC
TXD0
TXD1
TXD2
NC#N5
NC#N4
NC#N3
NC#N2
NC#R3
NC#R2
NC#R1
NC#T1
NC#T3
NC#T2
GPIO15
N15S-GT-S-A2-GP
VGA1I
9 OF 14
IFPD
NC#U6
NC#T7
NC#R7
NC#R6
I2CX_SDA
I2CX_SCL
NC#P4
NC#P3
NC#R5
NC#R4
NC#T5
NC#T4
NC#U4
NC#U3
NC#V4
NC#V3
GPIO17
N15S-GT-S-A2-GP
VGA1J
10 OF 14
IFPEF
IFPE
IFPF
NC#J7
NC#K7
NC#K6
NC#H6
NC#J6
DVI-DL
DVI-SL/HDMI
I2CY_SDA
I2CY_SCL
NC#J3
NC#J2
NC#J1
NC#K1
NC#K3
NC#K2
NC#M3
NC#M2
NC#M1
NC#N1
NC FOR GK208
HPD_E
GPIO18
NC FOR GF117
I2CZ_SDA
I2CZ_SCL
NC#H4
NC#H3
NC#J5
NC#J4
NC#K5
NC#K4
NC#L4
NC#L3
NC#M5
NC#M4
HPD_F
GPIO19
VGA1K
11 OF 14
DACA
NC#W5
NC#AE2
NC#AF2
TSEN_VREF
GM108/GK208
I2CA_SCL
I2CA_SDA
NC#AE3
NC#AE4
NC#AG3
NC#AF4
NC#AF3
GM108
GF117
GK208
RN7401
SRN1K8J-GP
20141012 SC - Terry
UMA
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Title
GPU_DIGITALOUT (2/5)
Size
A3
Document Number
Laduree-BDW 15.6"
Rev
1
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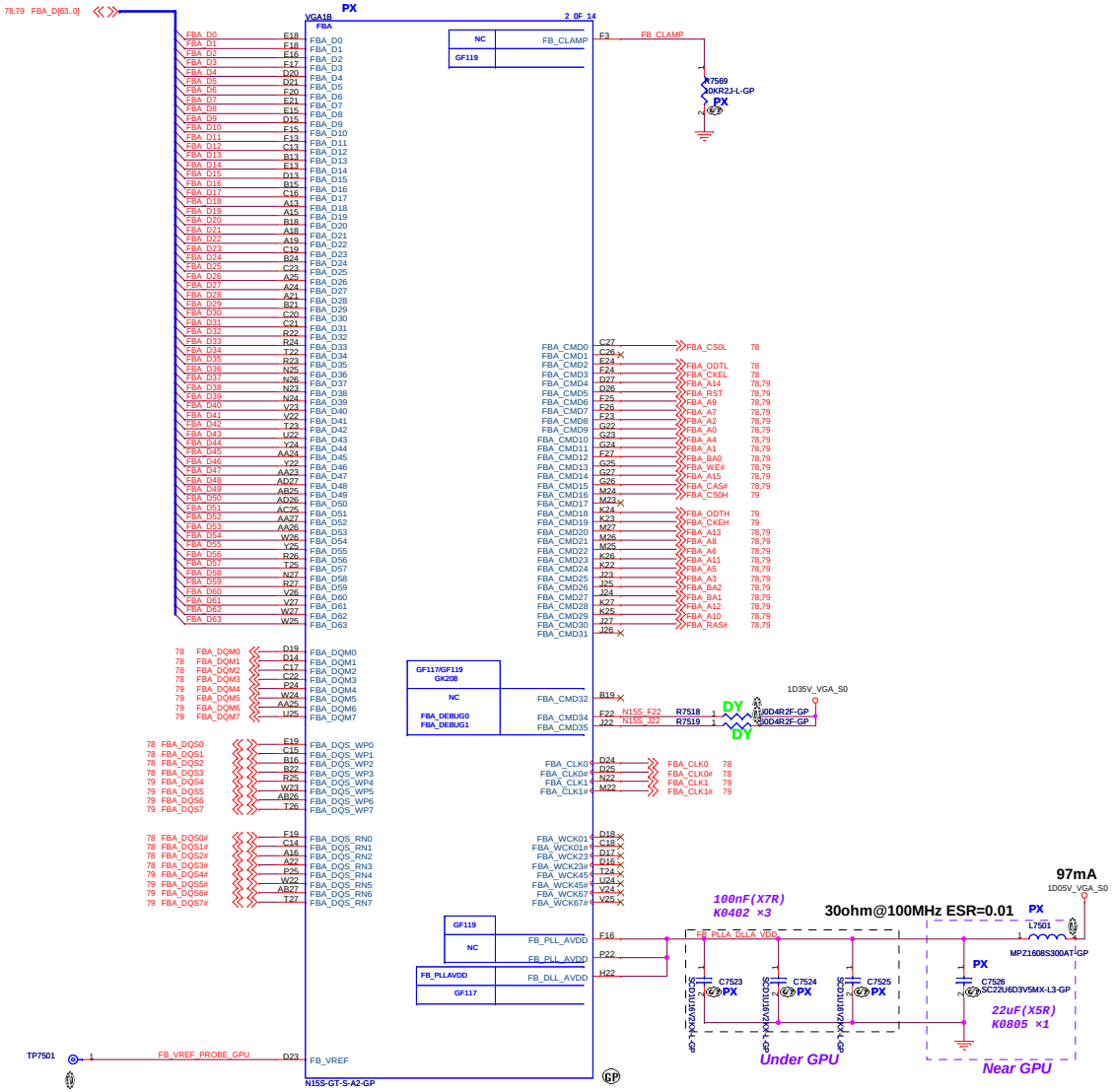

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Title: GPU_VRAM I/F (3/5)

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Custom	Laduree-BDW 15.6"	1

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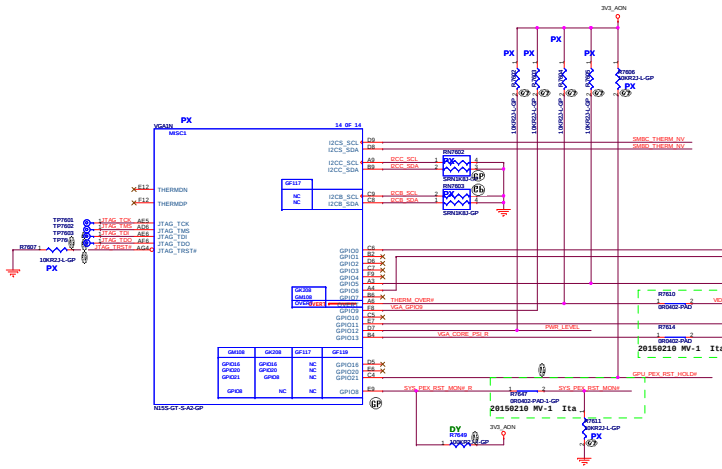
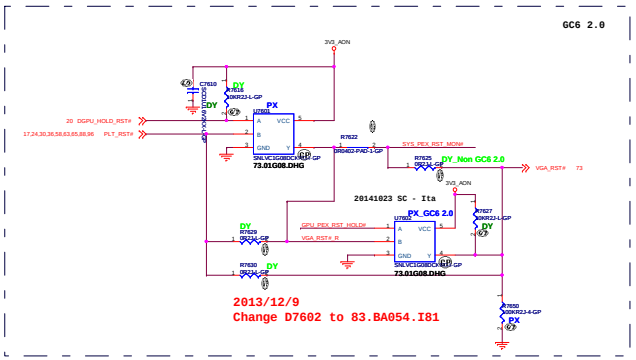
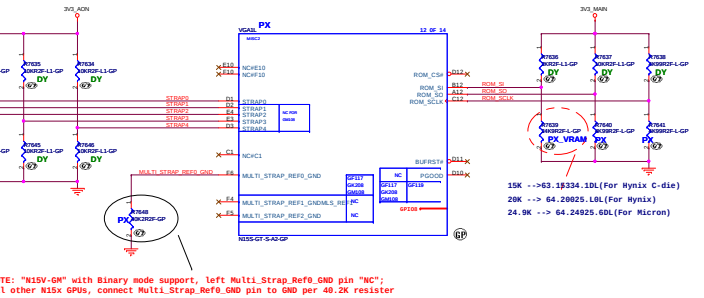






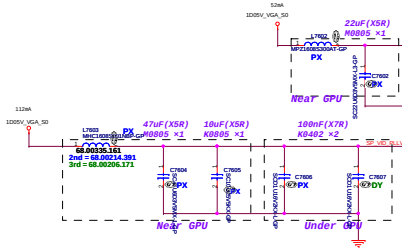
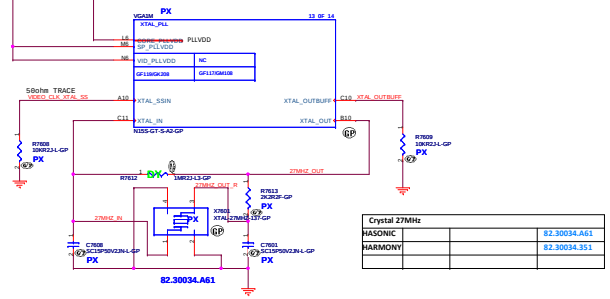
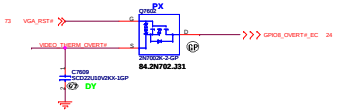


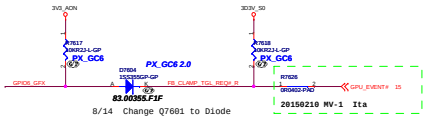
Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 µF	X7R	0402	1 per ball	Under GPU
		10 µF	X5R	0603	1	Near GPU
		47 µF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU



Crystal 27MHz			
HASONIC			82.30034.A61
HARMONY			82.30034.351





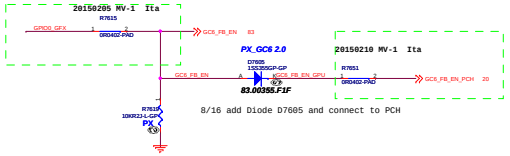


Table 4. N16S-GM/-GT/-LP DDR3L Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status	
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FFR-11C	F-die	0x9	900	N/A	Production candidate	
				Micron	MT41J128M16JT-093G:K	K-die	0xA	900	1322	Production candidate	
				Samsung	K4W2G1646Q-BC1A	Q-die	0xB	900	N/A	Production candidate	
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production candidate	690995-364
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production candidate	690995-662
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production candidate	
			Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production candidate	
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production candidate	
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production candidate	

C_die 0X2

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND	
4.99 kΩ	1000	0000	
10.0 kΩ	1001	0001	
15.0 kΩ	1010	0010	63.15334.1DL
20.0 kΩ	1011	0011	
24.9 kΩ	1100	0100 072.41256.0B0U	64.24925.6DL
30.1 kΩ	1101	0101	
34.8 kΩ	1110	0110	
45.3 kΩ	1111	0111	

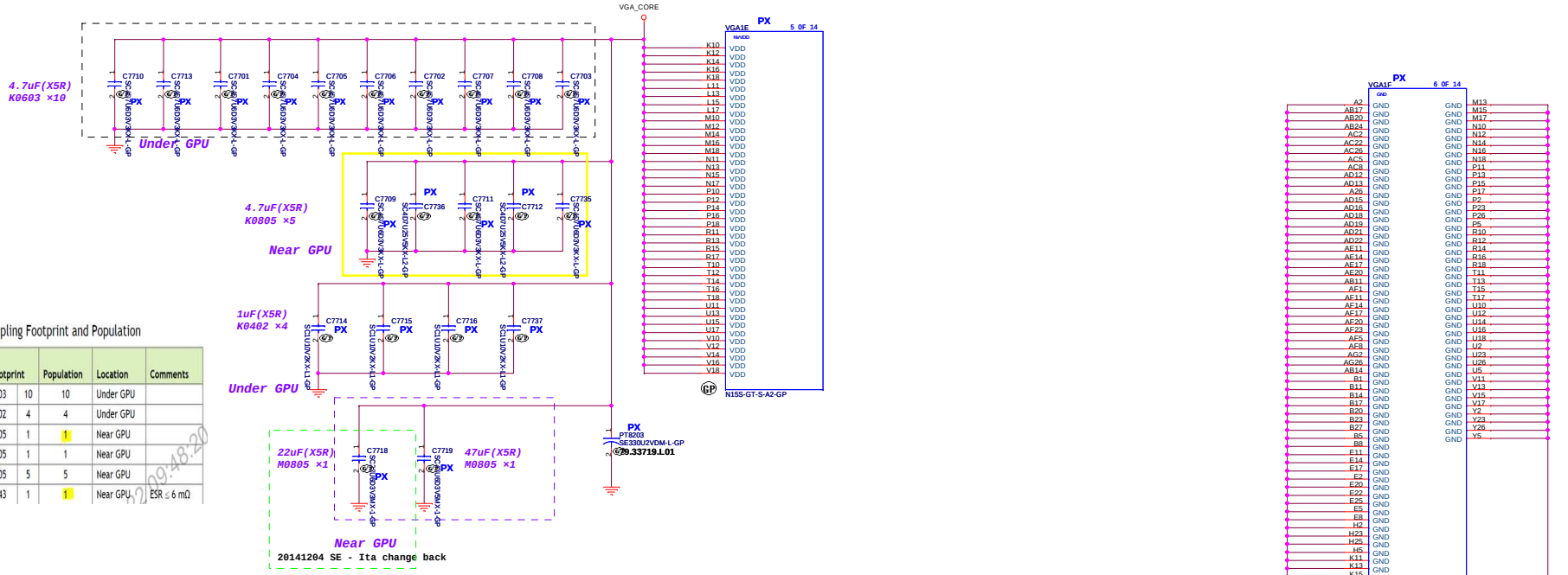


Table 3-6. NVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

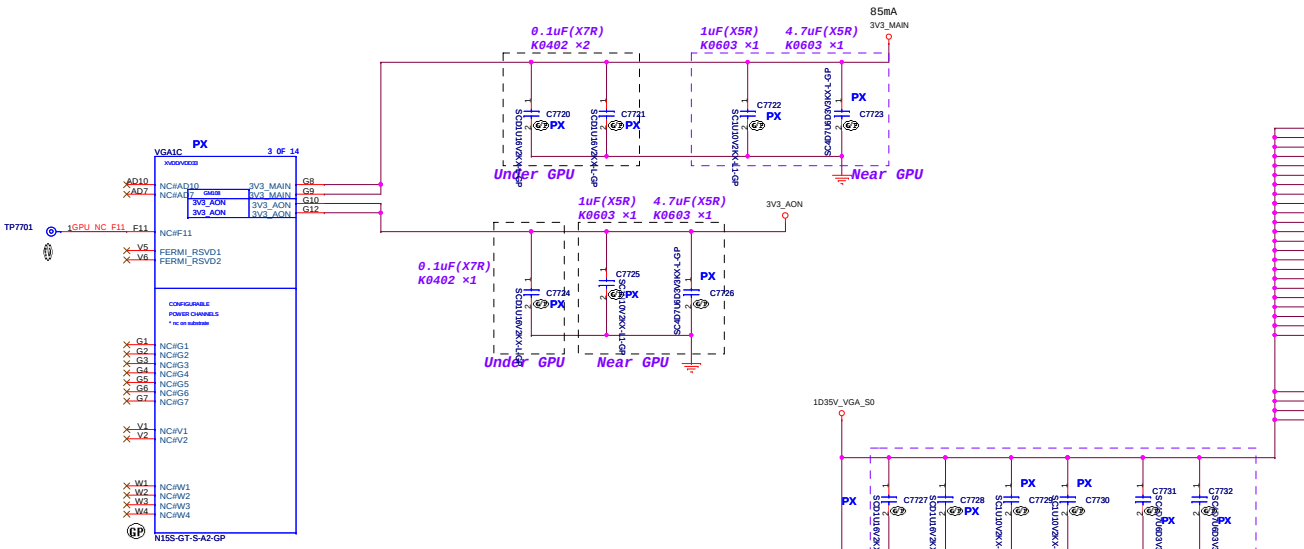
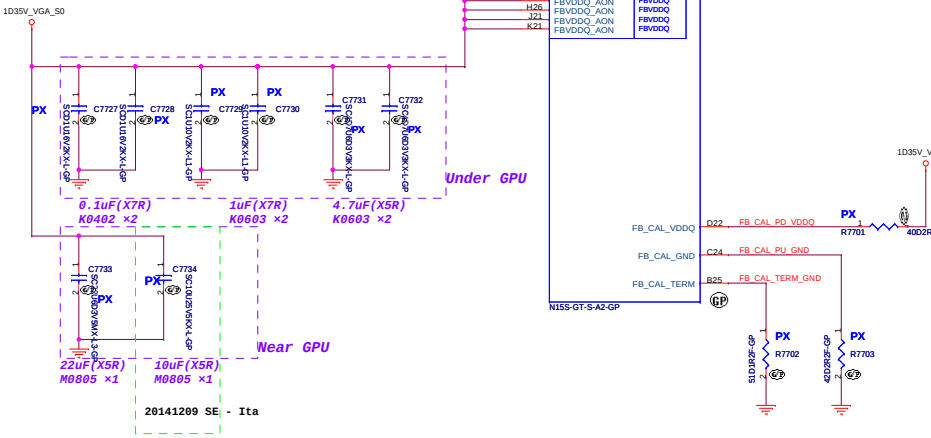


Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU



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Title: GPU_POWER/GND (5/5)

Size: A2 | Document Number: Laduree-BDW 15.6" | Rev: 1

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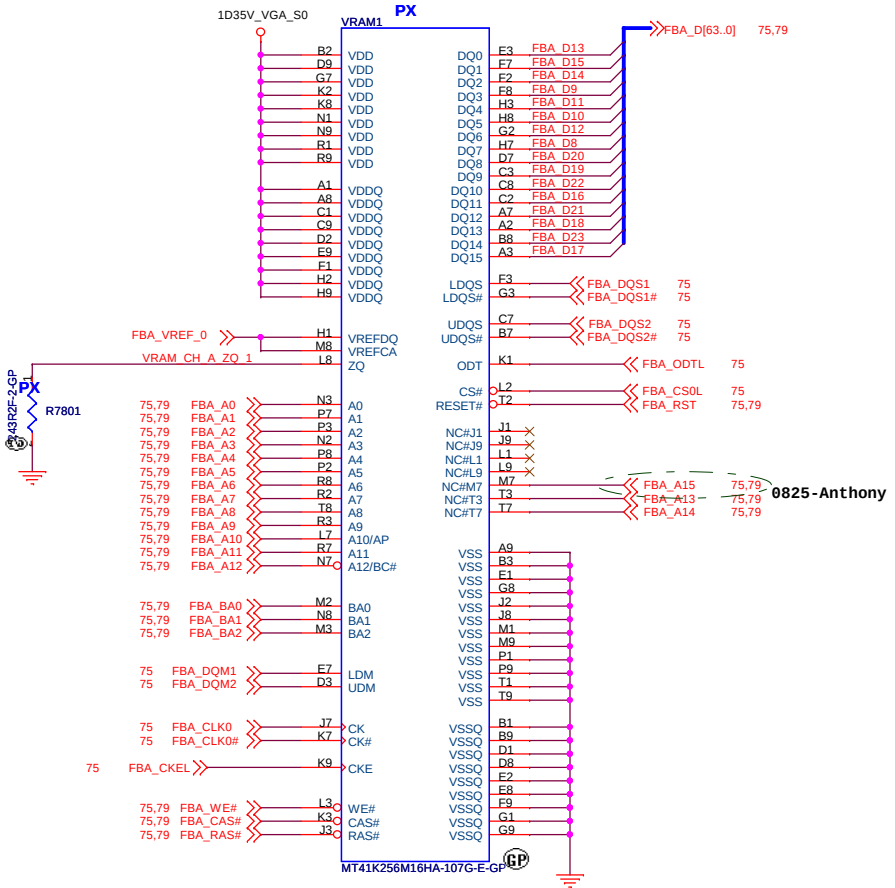

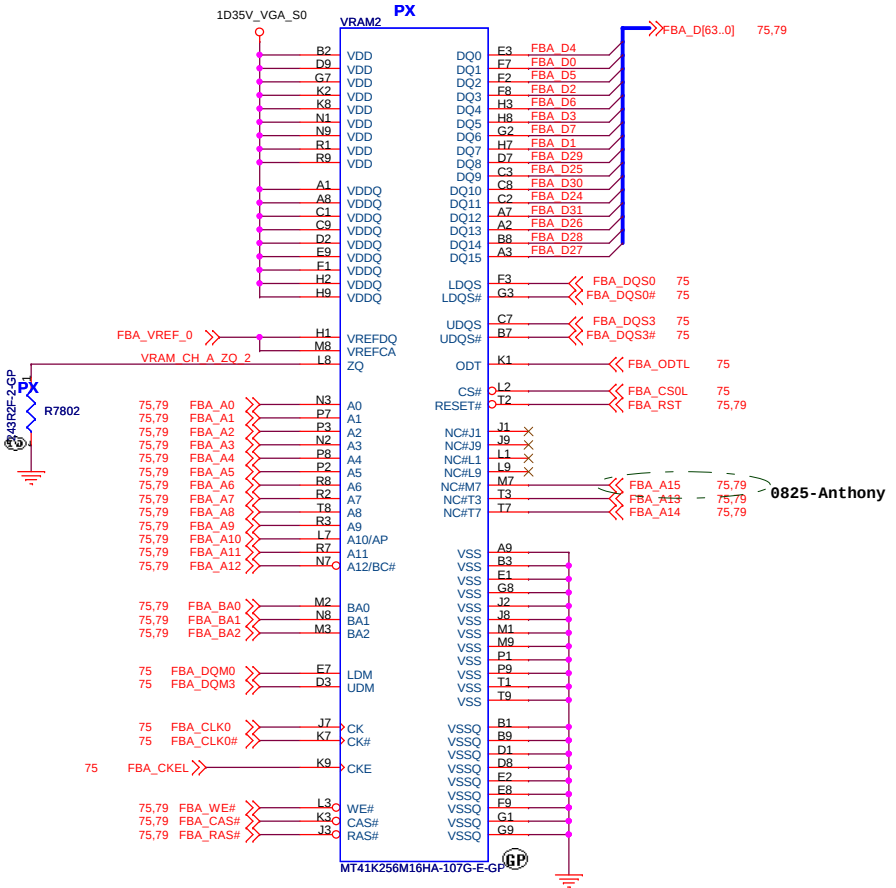

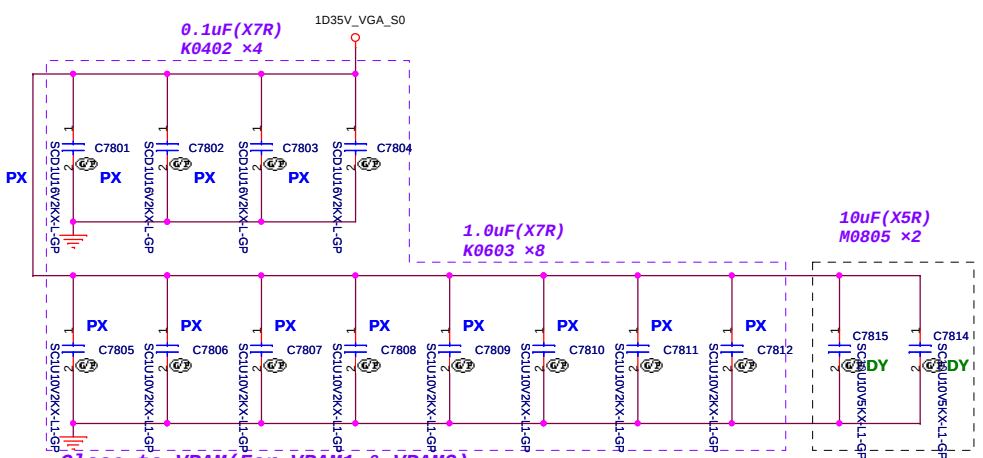

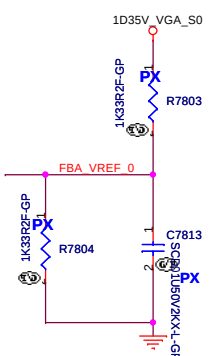

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Title: GPU-VRAM1,2 (1/2)		
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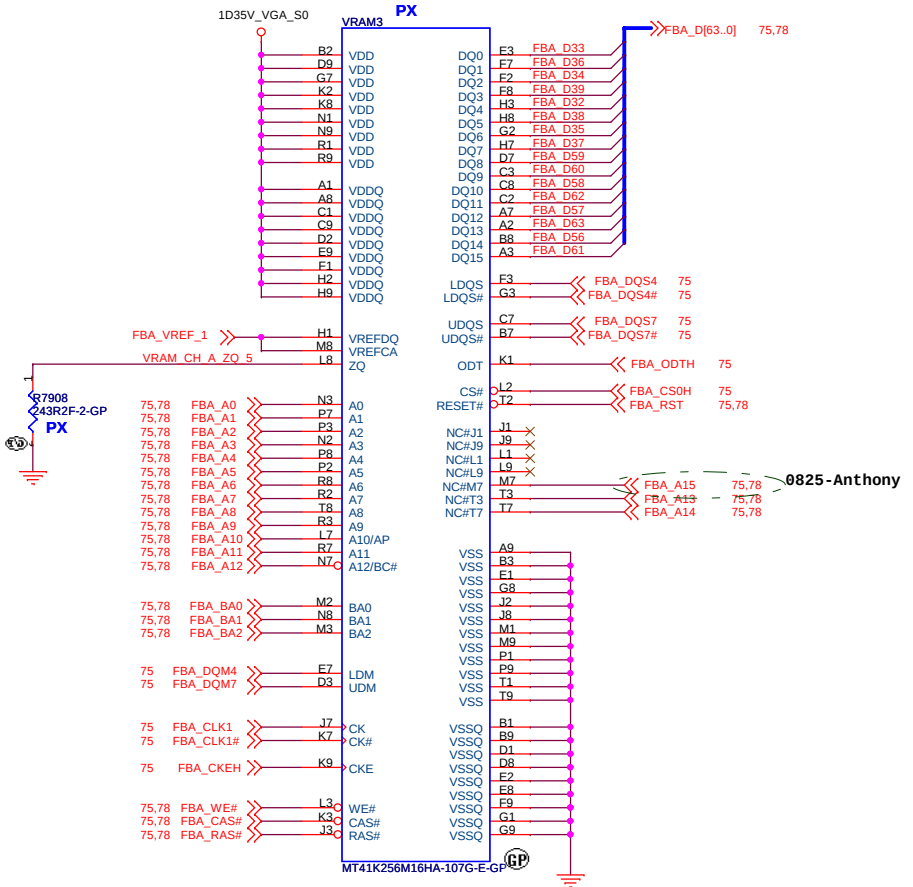

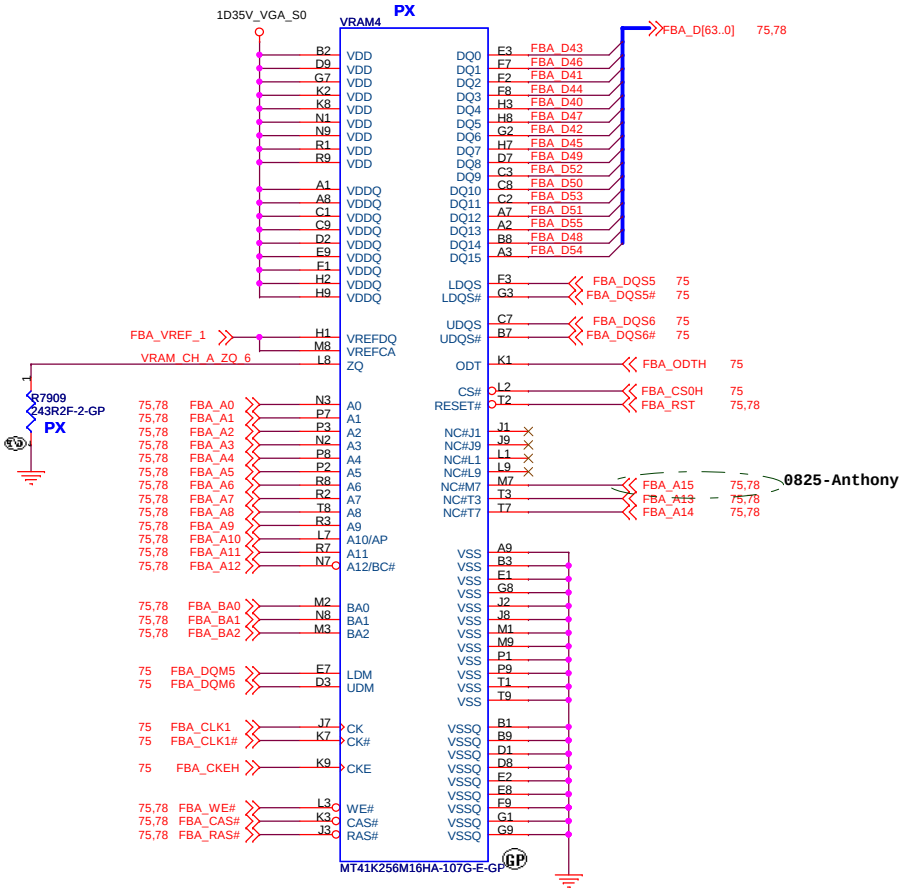

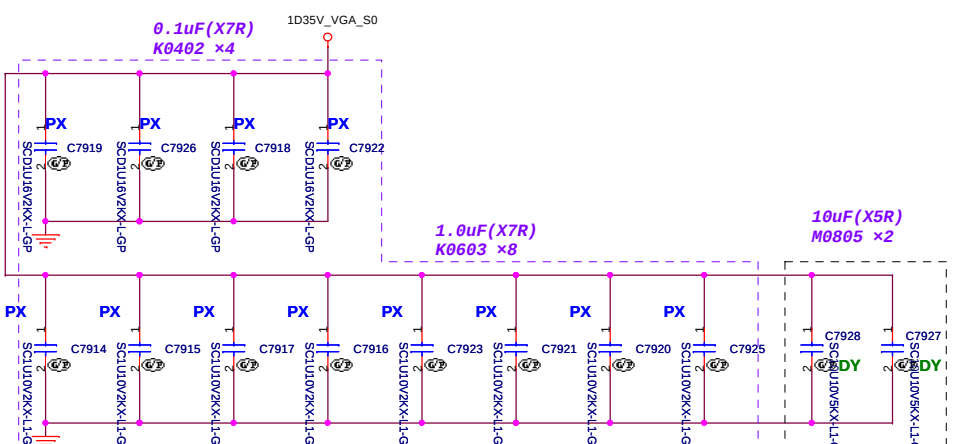

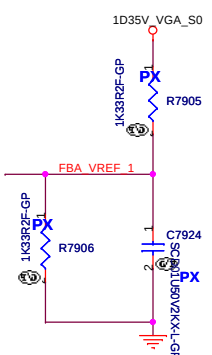

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Title: GPU-VRAM3,4 (2/2)		
Size: A3	Document Number: Laduree-BDW 15.6"	Rev: 1
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RT8179A_VGACORE(1/2)

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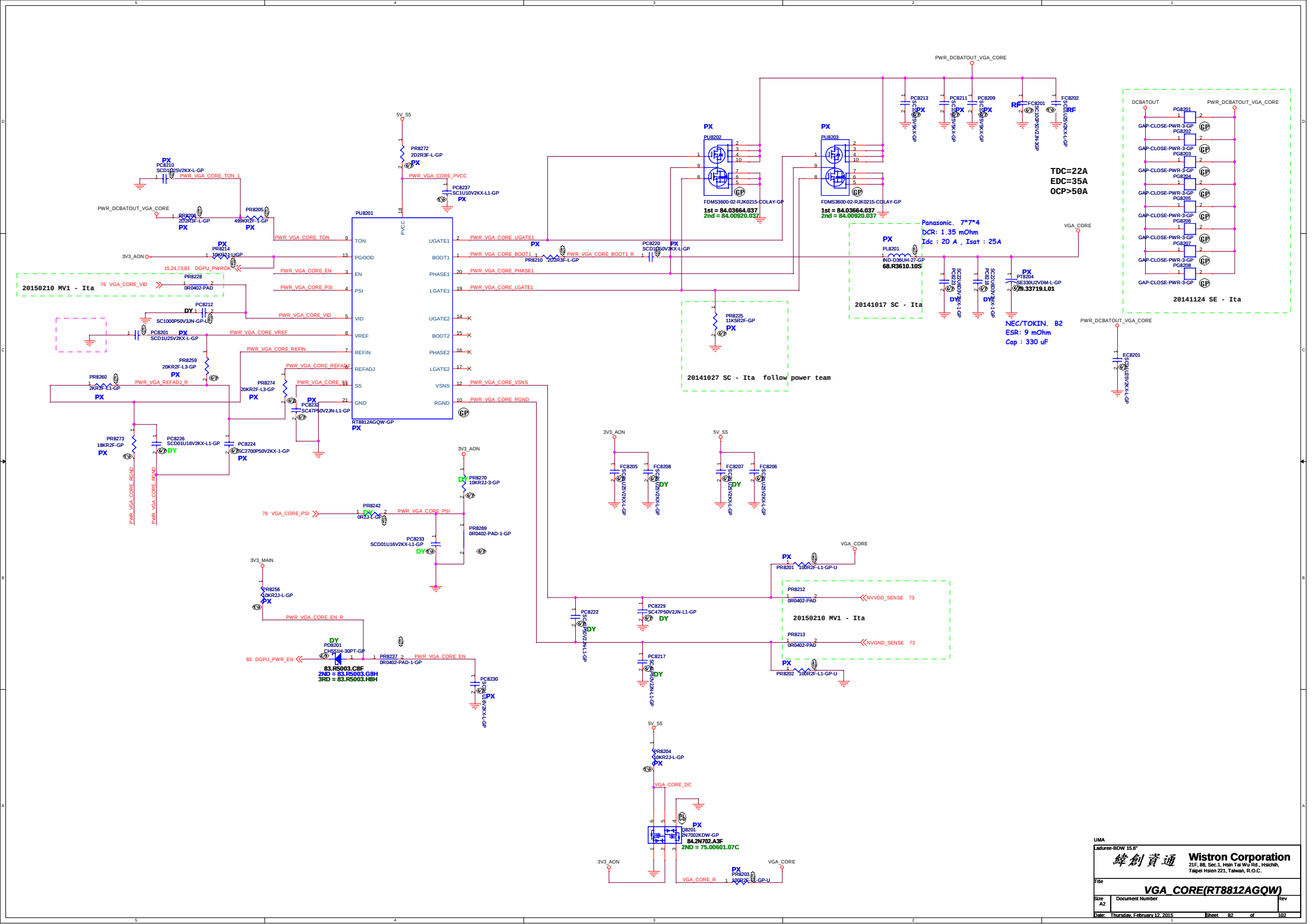
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RT8812AGQW-GP
PU8202
PU8203
FDMS3600-02-RJK0215-COLAY-GP
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2nd = 84.00920.037
TDC=22A
EDC=35A
OCP>50A
Panasonic, 7*7*4
DCR: 1.35 mOhm
Idc : 20 A , Isat : 25A
PL8201
IND-D36UH-27-GP
68.R3610.10S
NEC/TOKIN, B2
ESR: 9 mOhm
Cap : 330 uF
PT8204
20.33719.L01
VGA_CORE
20150210 MV1 - Ita
20141017 SC - Ita
20141027 SC - Ita follow power team
20141124 SE - Ita
DCBATOUT
PWR_DCBATOUT_VGA_CORE
3V3_AON
3V3_MAIN
5V_S5
VGA_CORE_DC
PWR_VGA_CORE_PVCC
PWR_VGA_CORE_TON
PWR_VGA_CORE_EN
PWR_VGA_CORE_PSI
PWR_VGA_CORE_VID
PWR_VGA_CORE_VREF
PWR_VGA_CORE_REFIN
PWR_VGA_CORE_REFADJ
PWR_VGA_CORE_SS
PWR_VGA_CORE_UGATE1
PWR_VGA_CORE_BOOT1
PWR_VGA_CORE_PHASE1
PWR_VGA_CORE_LGATE1
PWR_VGA_CORE_VSNS
PWR_VGA_CORE_RGND
NVVDD_SENSE
NVGND_SENSE
DGPU_PWR_EN
VGA_CORE_R
TON
PGOOD
EN
PSI
VID
VREF
REFIN
REFADJ
SS
GND
UGATE1
BOOT1
PHASE1
LGATE1
UGATE2
BOOT2
PHASE2
LGATE2
VSNS
RGND
PVCC
Ladurée-BDW 15.6"
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VGA_CORE(RT8812AGQW)
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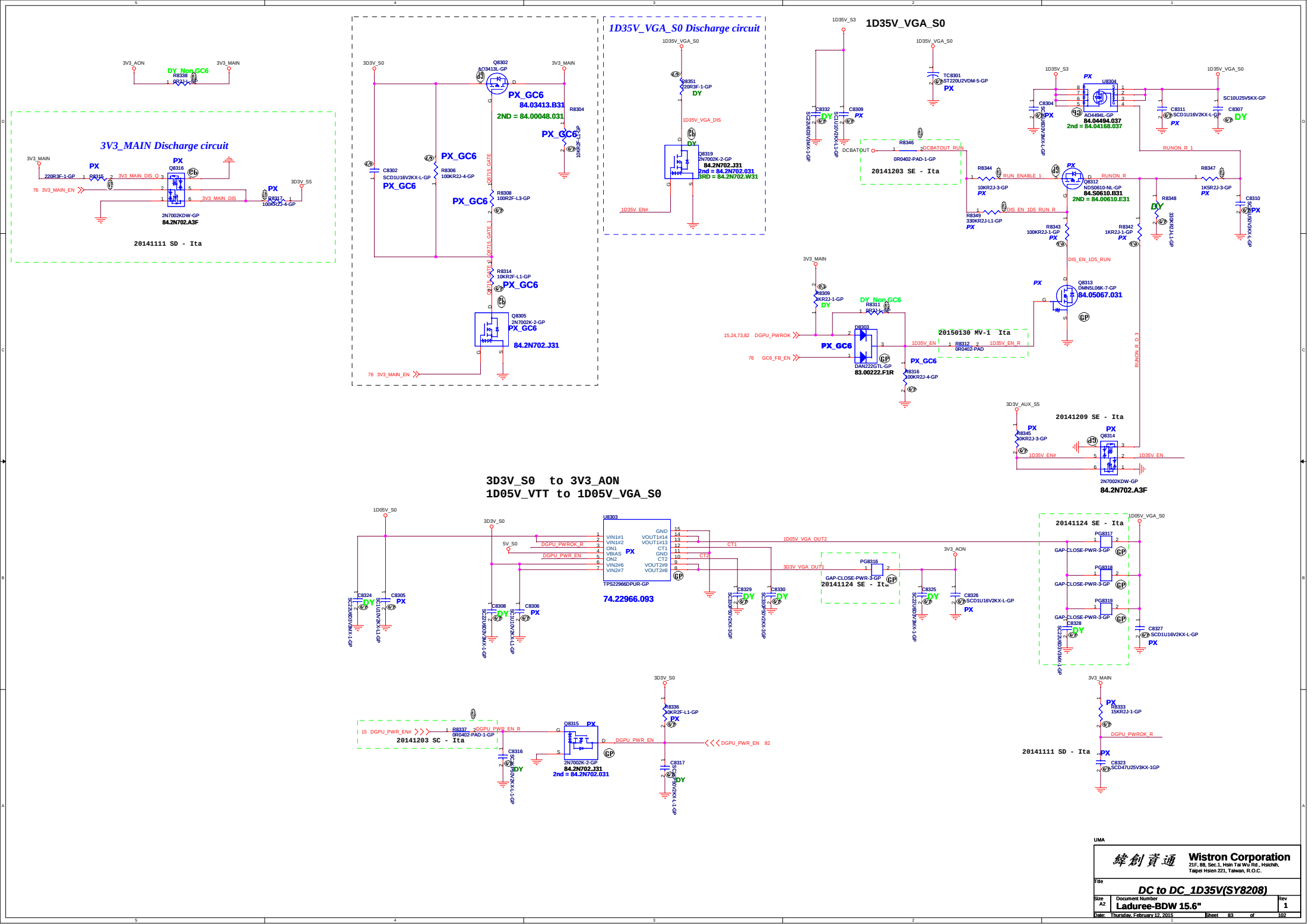
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1D35V_VGA_S0 Discharge circuit
1D35V_VGA_S0
3D3V_S0 to 3V3_AON
1D05V_VTT to 1D05V_VGA_S0
20141111 SD - Ita
20141203 SE - Ita
20150130 MV-1 Ita
20141209 SE - Ita
20141124 SE - Ita
20141203 SC - Ita
20141111 SD - Ita
Wistron Corporation
DC to DC_1D35V(SY8208)
Laduree-BDW 15.6"

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DISCRETE VGA POWER

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Title

Switchable GFX LCD(2/2)

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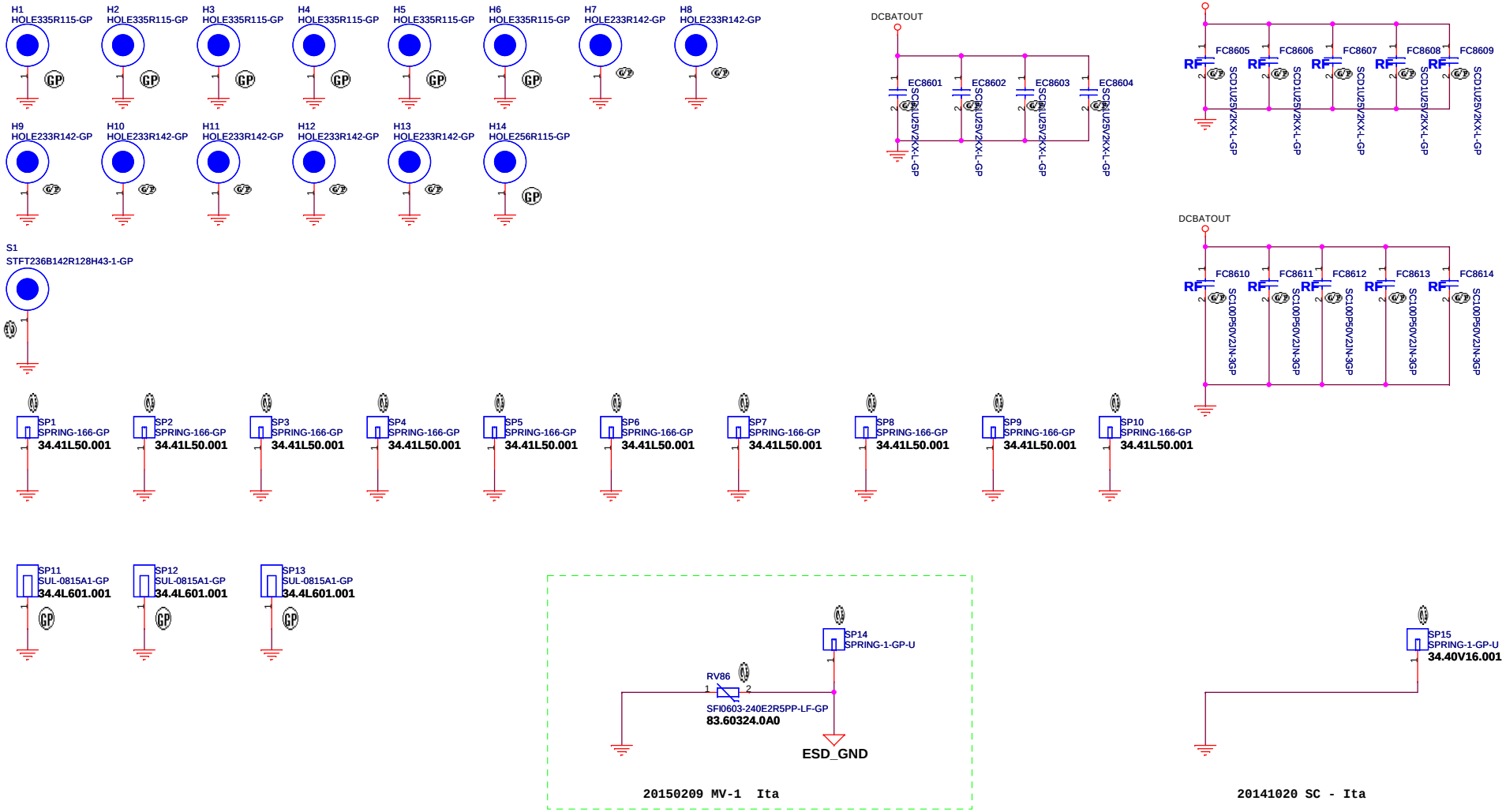

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Title: ***UNUSED PARTS/EMI Capacitors***

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A3	Laduree-BDW 15.6"	1

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Title: ***NFC***

Size	Document Number	Rev
Custom	**Laduree-BDW 15.6"**	1

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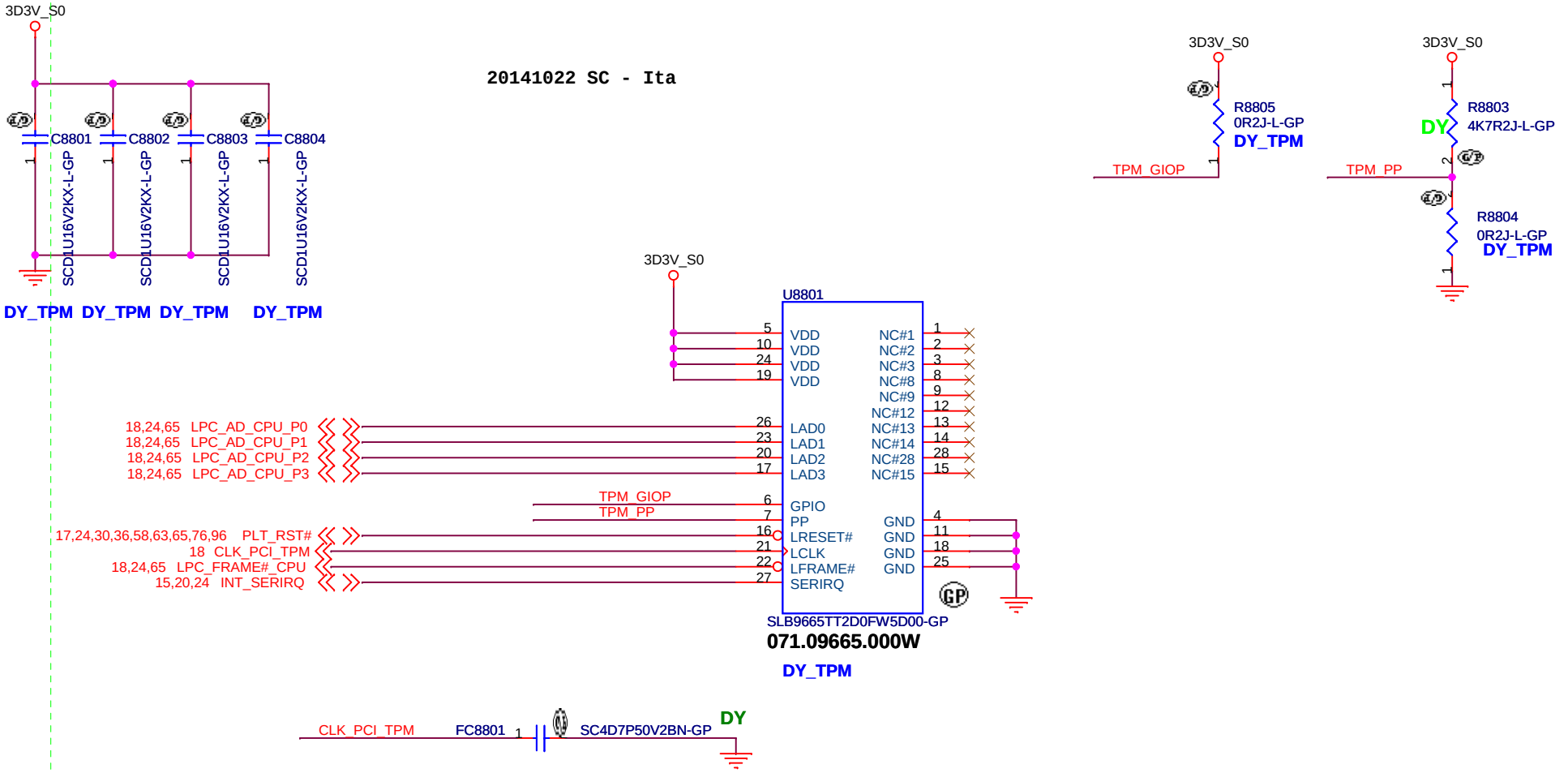

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Title: **TPM**

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A4	Laduree-BDW 15.6"	1

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Title

Finger Print

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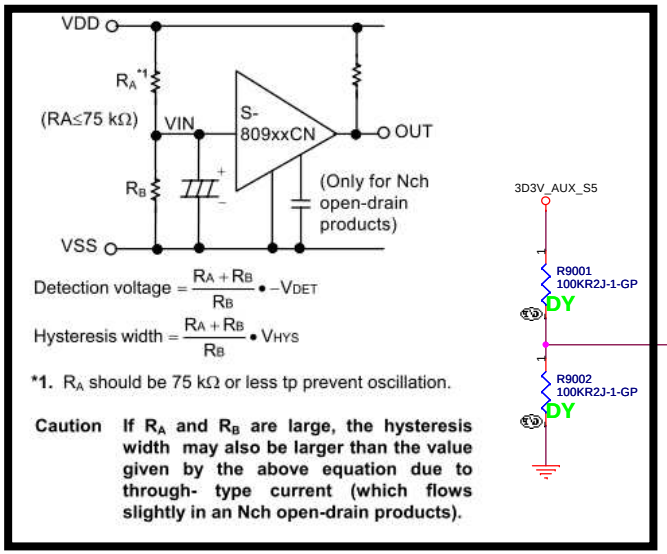

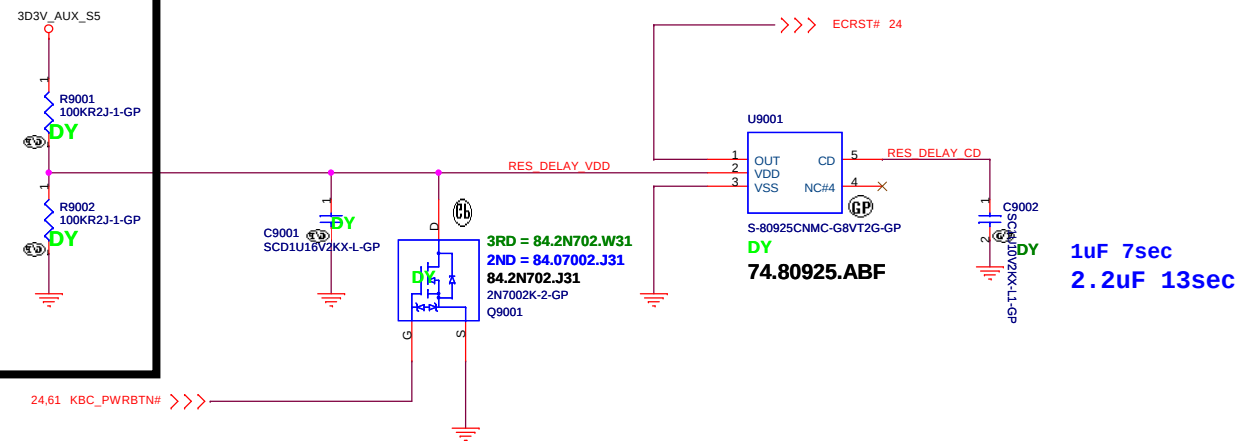

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Title	***Battery Reset***	
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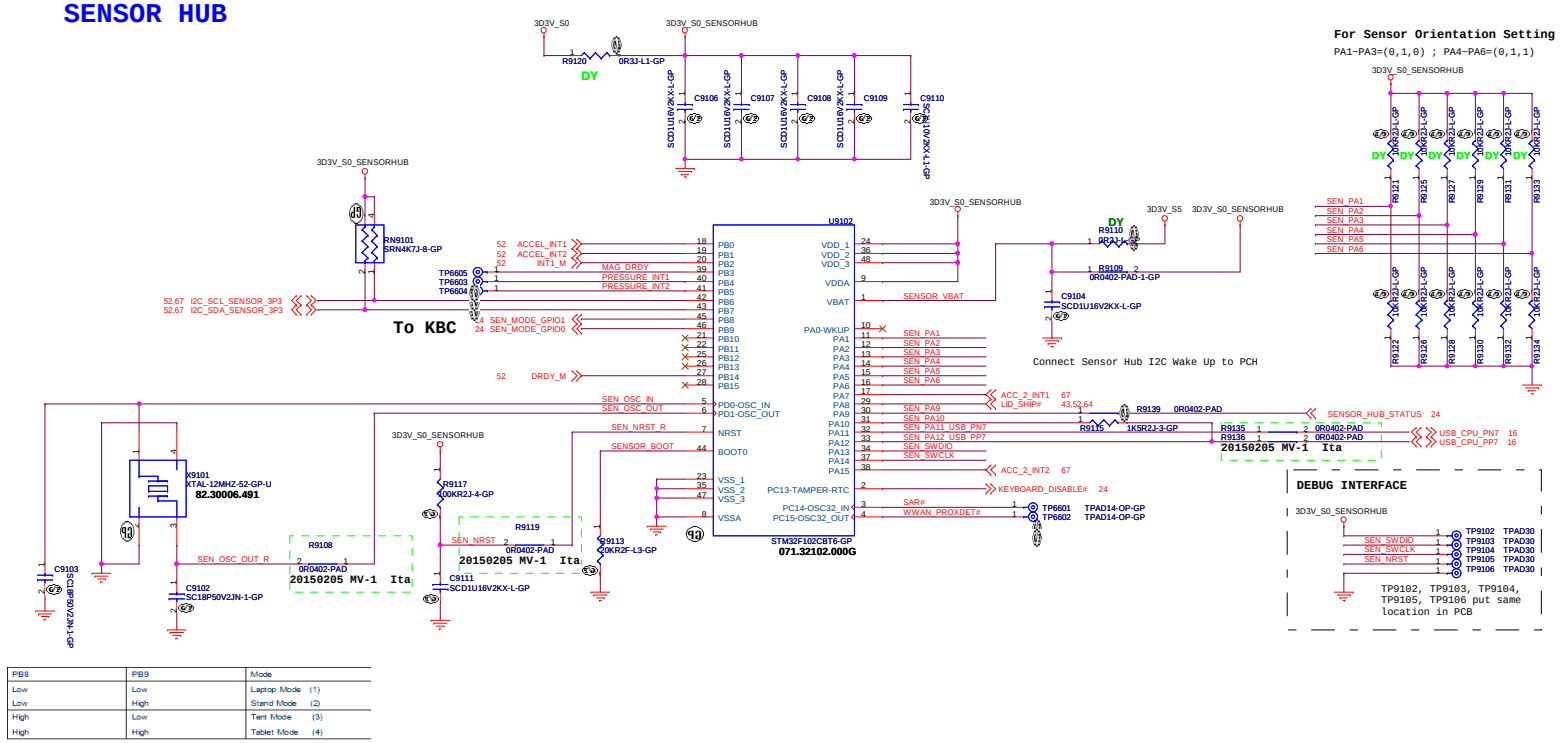
SENSOR HUB

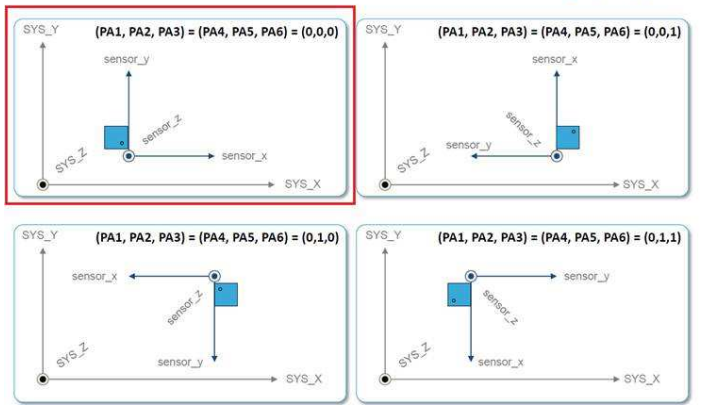


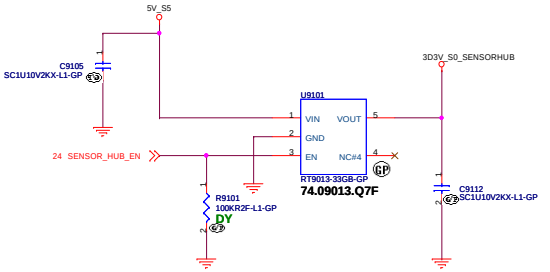
PB8	PB9	Mode
Low	Low	Laptop Mode (1)
Low	High	Stand Mode (2)
High	Low	Tent Mode (3)
High	High	Tablet Mode (4)

According to HP request for lid angle detect during S3 mode. We are need to add new GPIO from EC to MCU PA9 to inform sensor hub current status of OS. We may need to refer this signal for periodically wake up to detect lid angle during S3 state.

OS mode (Sensor hub Powered)	PA9 (Normal Low) from EC
S0	Low
S3	High

LSM9DS1 Orientation Setting (Top)





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Title: Sensor HUB

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Switchable GFX eDP

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Title

Bottom Docking

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Inter LAN WG1217LM

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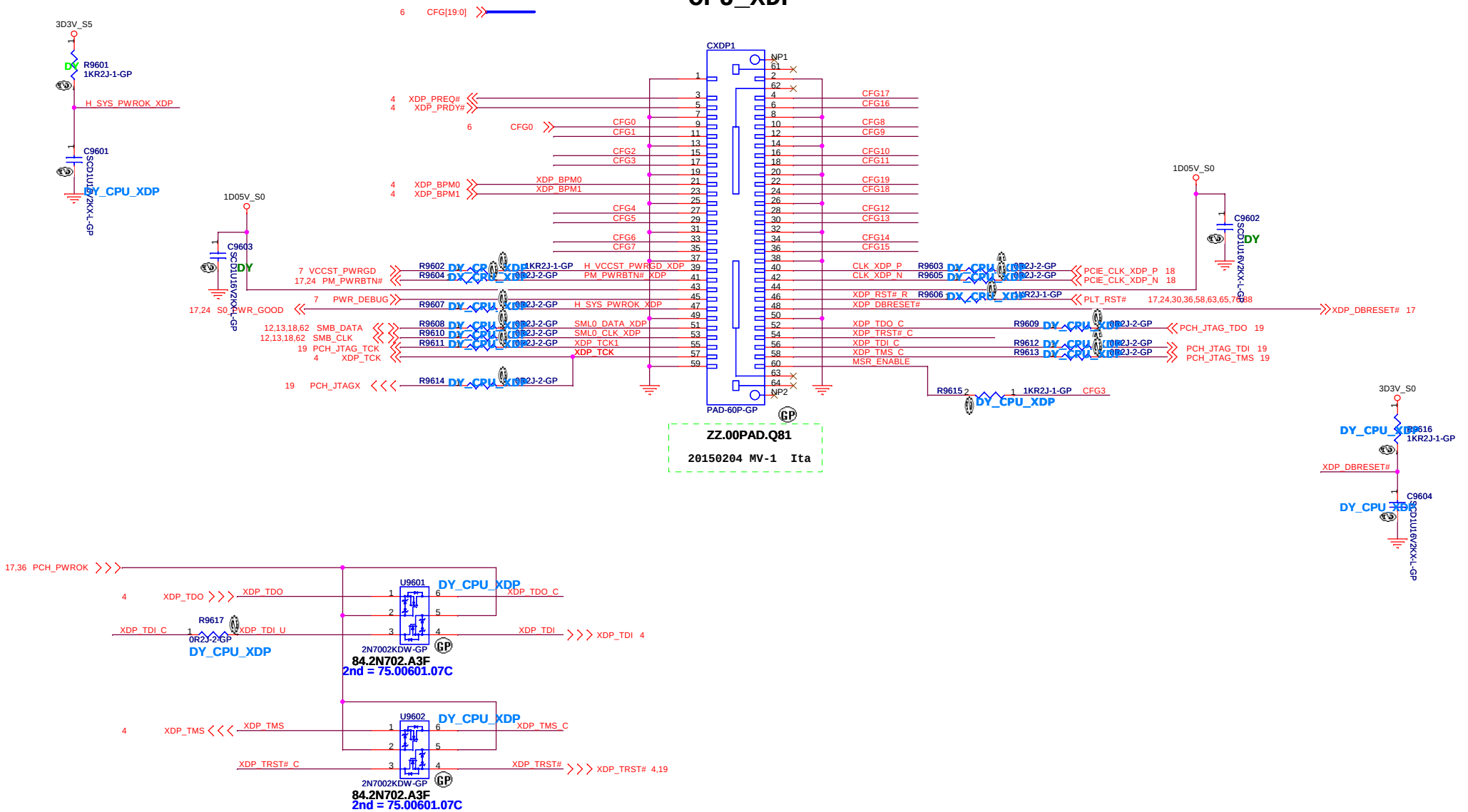
CPU_XDP



Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	O	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title

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2nd list 20150205 update
All parts follow this list

Part Number	2nd	3rd	Manual PN
71.BROAD.00U			790141-001
071.0N15S.0A0U			796748-001
72.41K26.00U			690995-662
022.10025.00A1	22.10296.211		
20.F0818.004	020.F0243.0004	020.F0281.0004	
20.K0678.044	20.K0809.044		
20.K0637.014			
20.K0848.030	20.K0809.030		
062.10011.0461	710882-AD4	677746-DD4	677746-FD4
062.10011.0841	62.10024.N21	062.10011.00A1	661678-302
022.10005.00U1	022.10005.01H1		
020.K0044.0012	020.K0125.0012	020.K0049.0012	
62.10043.P21	735274-AE2	735274-LE2	735274-FE2
20.K0800.004	20.K0841.004		
020.K0116.0032	020.K0137.0032		
20.k0823.006	020.K0048.0006		
062.10007.0451	734729-AB2		734729-FB2
022.10001.00D1			022.10001.00R1
75.00054.R7D	75.BAT54.07D	83.BA54A.A81	
75.04223.07C	075.01256.007C		75.00005.C7C
83.00016.F11	83.00016.P11		83.00016.I11
83.00040.E81	83.R2004.C81	83.00040.T81	
83.00099.U11	83.BAV99.I11		
83.0024V.0A1	75.04024.07D	83.03024.0A1	
83.00355.F1F	83.00355.D1F	83.00355.G1F	
83.00751.08F	83.R2004.G8F		
83.R2003.P8F	83.R2003.A8M		
83.R5003.C8F	83.R5003.T8F		83.R5003.H8H
83.00222.F1R			83.00222.B1R
84.00043.011	084.05233.001H	84.05143.011	
84.00124.H1K	84.00024.A1K	84.05212.B11	
84.00124.K1K	84.00024.01K		
84.02222.V11	084.02222.0011		
84.03904.L06	84.03904.E11		
84.T3904.H11	084.03904.0B11		
84.T3906.A11	84.M3906.B11	84.T3906.E11	
82.30004.841	82.30004.891		
82.30006.491	82.30006.641		
82.30020.G71	82.30020.D41		
82.30034.A61	82.30034.351		
84.02305.G31	84.02305.I31		
84.03413.B31	84.02130.031	84.00102.031	
84.04494.037	84.04168.037		
84.05067.031	84.00301.A31		
84.2N702.A31	084.27002.0B31	84.2N702.031	
84.2N702.A3F	075.27002.0A7C	84.00512.03F	
84.2N702.J31	084.07002.0C31		
84.S0610.B31	84.00610.E31		
83.00222.F1R			83.00222.B1R
69.50007.A41	69.50007.A31		
73.01G08.DHG	73.01G08.EHG	073.7SZ08.000H	
74.02821.07F	074.05243.007F		
74.09724.09F	74.06288.B7F	74.03514.07F	
74.22966.093		074.22966.0093	
68.00084.921	68.00213.031	68.00217.401	
68.00143.051	68.00230.091	68.00335.101	
68.00212.051	68.00334.051	68.00335.051	
68.00335.161	68.00214.261	68.00206.171	
68.2R21D.10R	68.2R21G.10Q		
68.2R21G.10P	68.2R21G.10D	68.2R21A.20X	
68.R681A.10A	68.R6810.20J		
69.10103.041	69.10084.071	68.00201.141	
ZZ.00215.037			84.03664.037
84.08131.037	84.07403.037		
68.4R71C.10K	068.4R710.1081		
84.00780.037	84.07506.037		
68.3R310.20A	68.3R31C.10E		
74.01339.B3F	074.09198.0A3F		
69.60037.031	69.60028.011		
69.60037.011	69.60013.131		
79.33719.L01	77.53371.21L		
68.00069.30A	68.IH080.301		68.69241.301
72.25Q64.F01	72.25640.D01		
82.30001.G11	82.30001.G01		
74.09013.P7F	074.03705.003F		
68.R3610.10S	68.R3610.20D		
69.48001.081	69.50011.081		
077.51571.0001	077.51571.0021		
068.1R010.1081	68.1R01B.10K		
83.00056.Q11	83.00056.Y11	75.00056.I7D	
84.06414.037	84.00172.A37		
68.00213.011	68.00084.43A	68.00225.121	
75.01045.073	075.07504.0073		
071.08407.0003			71.08201.G03
78.10421.L0L			78.10422.L1L
83.05123.AA0	83.3V3XU.AA0		
75.00099.O7D	75.00099.K7D		

7" Reel	13"Reel
78.10134.1FL	78.10134.L1L
78.10324.2FL	78.10324.L0L
78.10610.5BL	78.10610.L0L
78.22523.5BL	78.22523.L1L
78.22610.51L	78.22610.L2L
78.47520.5BL	78.47520.L0L
63.00000.00L	63.R0033.L0L
63.10234.1DL	63.10234.L0L
63.10334.1DL	63.10334.L0L
63.10434.1DL	63.10434.L1L
63.33034.1DL	63.33034.L0L
63.47234.1DL	63.47234.L0L
63.47334.1DL	63.47334.L0L
63.47434.1DL	63.47434.L0L
63.56034.1DL	63.56034.L0L
63.R0034.1DL	63.R0034.L0L
64.10015.6DL	64.10015.L3L
64.10025.6DL	64.10025.L0L
66.10336.04L	66.10336.L0L
66.22236.04L	66.22236.A4L
78.47522.51L	78.47522.L4L
78.10424.2BL	78.10424.L0L
78.10523.5FL	78.10523.L2L
78.10224.2FL	78.10224.L1L
78.10422.5FL	78.10422.L1L
78.22423.5FL	78.22423.L2L
64.10005.6DL	64.10005.L1L
63.22234.1DL	63.22234.L0L
63.22034.1DL	63.22034.L0L
64.20025.6DL	64.20025.L0L
64.15005.6DL	64.15005.L0L
64.10035.6DL	64.10035.L3L
64.2R205.55L	64.2R205.L0L
63.10534.1DL	63.10534.L1L
63.33434.1DL	63.33434.L1L
63.82234.1DL	63.82234.L0L
64.10R05.6DL	64.10R05.L1L
64.1R005.6DL	64.1R005.L0L
64.49R95.6DL	64.49R95.L0L
78.10034.1FL	78.10034.L0L
78.22224.2FL	78.22224.L0L
64.20005.6DL	64.20005.L0L
64.20035.6DL	64.20035.L4L
64.13005.6DL	64.13005.L0L
64.20015.6DL	64.20015.L0L
63.51034.1DL	63.51034.L0L
78.10622.51L	78.10622.L4L
78.22034.1FL	78.22034.L1L
78.47034.1FL	78.47034.L0L
63.22334.1DL	63.22334.L0L

0.1U 16V K0402 X7R change to 0.1U 25V K0402 X5R

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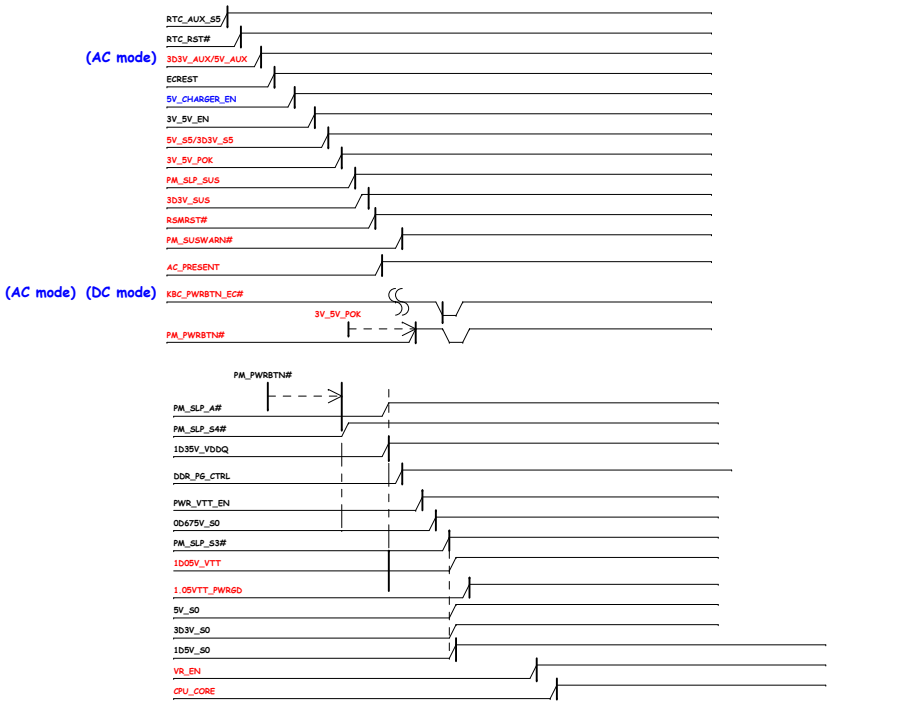
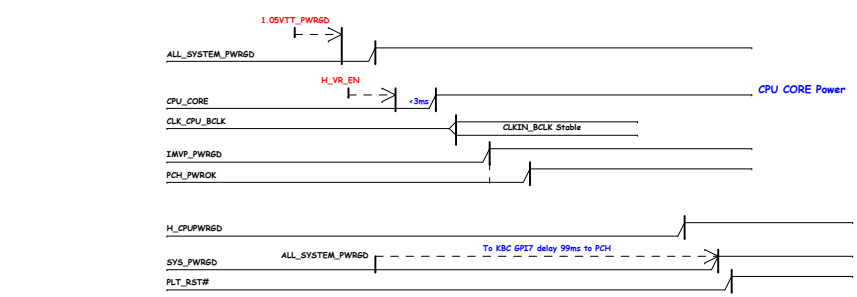
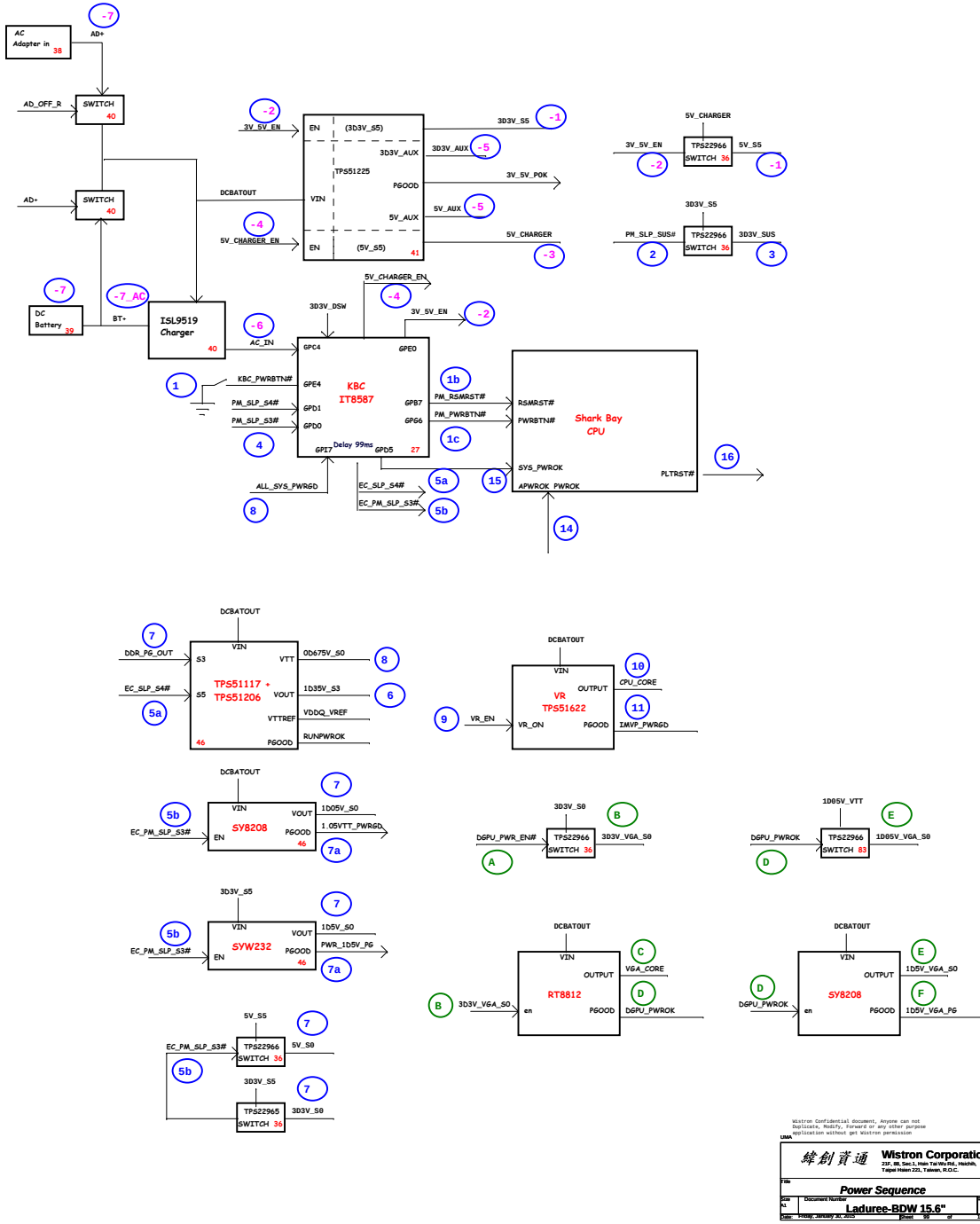
Intel-Power Up Sequence





SHARK BAY POWER UP SEQUENCE DIAGRAM



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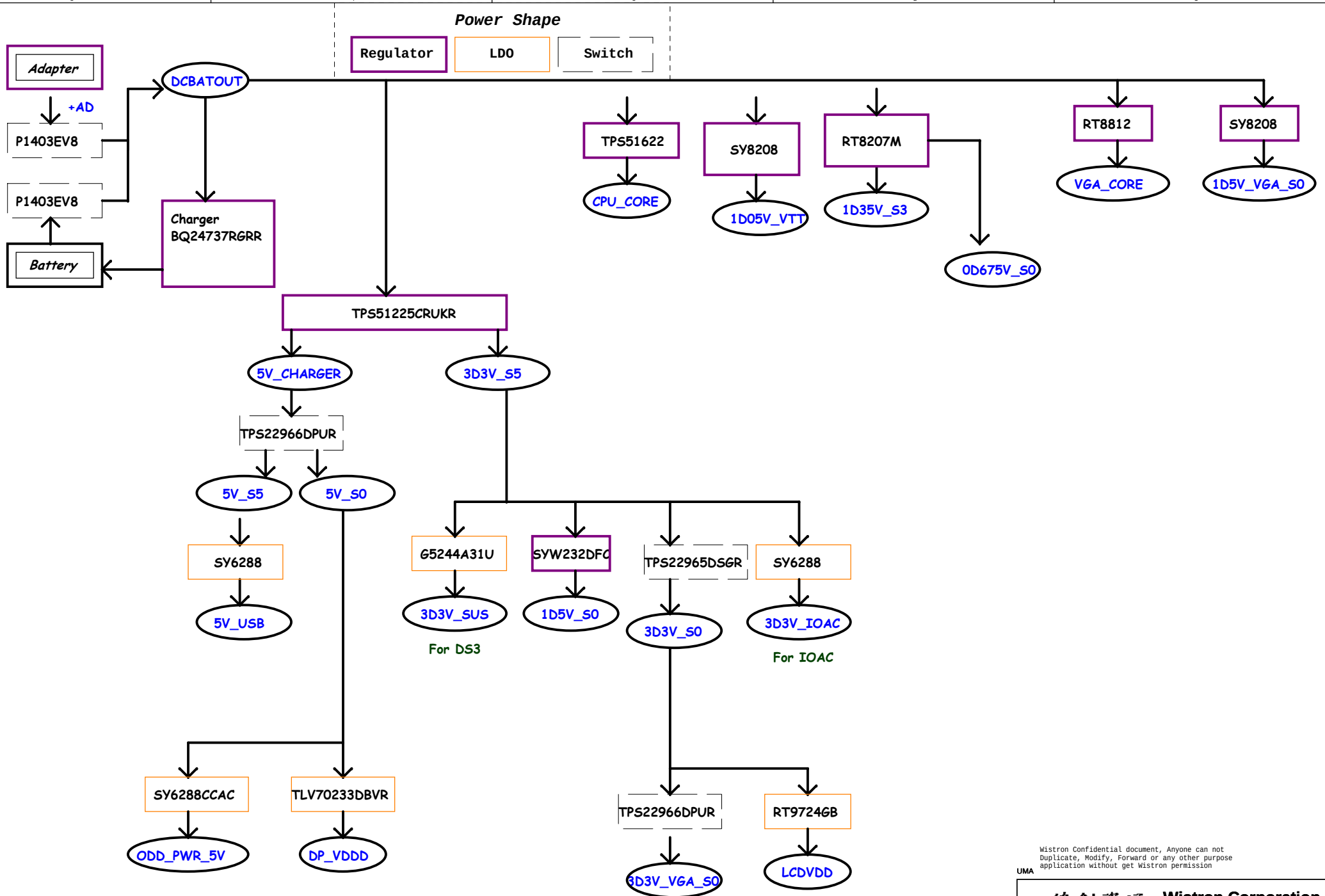

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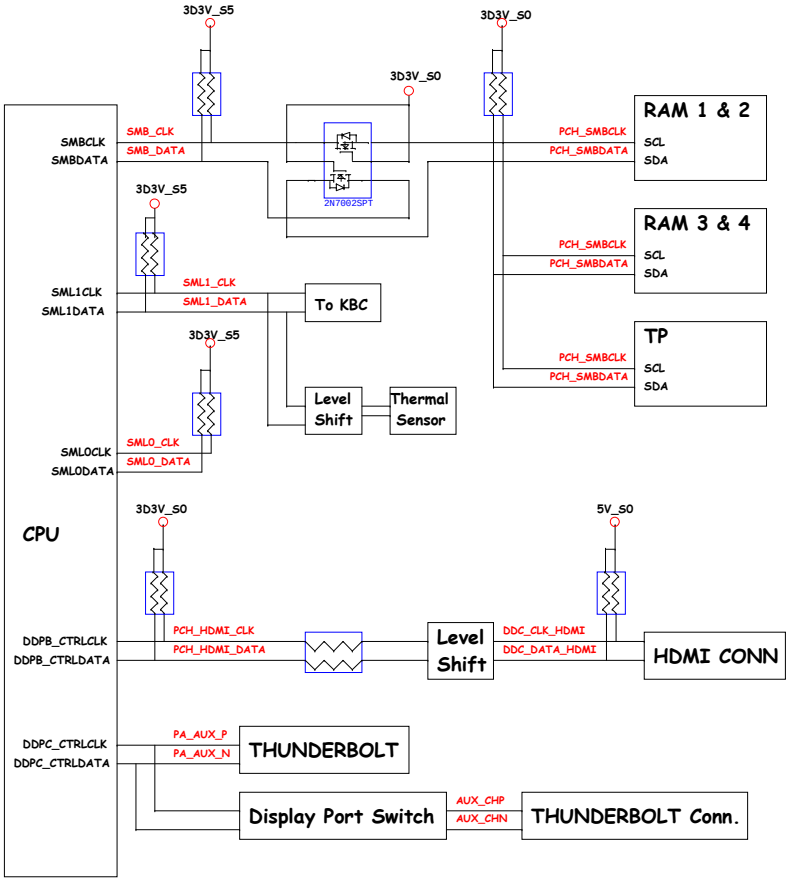
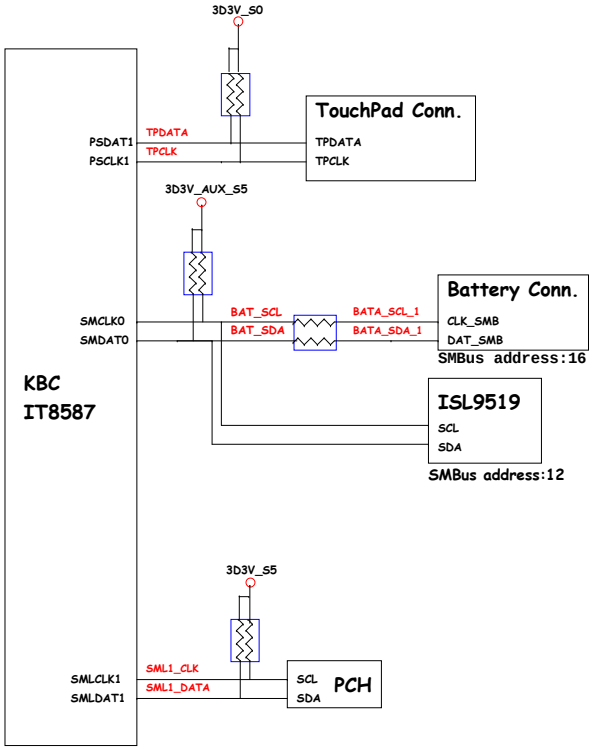
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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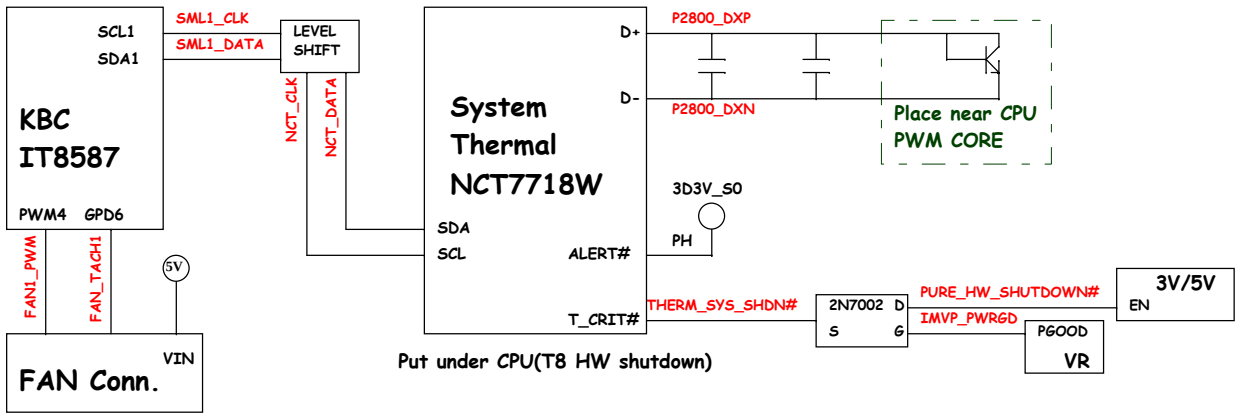
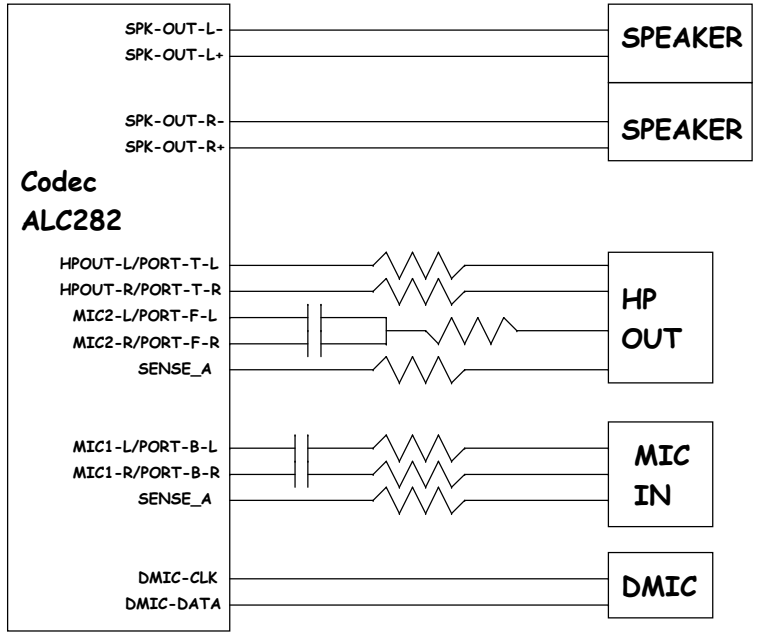
Thermal Block Diagram



Put under CPU(T8 HW shutdown)

Audio Block Diagram



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Title: **THERMAL/AUDIO BLOCK DIAGRAM**

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